Binary Representation of DOM Raw Engineering Event

Version 1.6
Covers Event Formats 1 and 2
10/20/05

C. McParland, J. Jacobsen, D. Hays

The following document describes a binary representation of the DOM Raw Engineering Event. A detailed description of the fields contained in this event can be found in other documents. The following describes a mapping of all data fields found in this event onto a single binary representation.

DOM Raw Engineering Event:
A binary formatted DOM "Raw Engineering Event" consists of the following blocks of binary data:

-Event Header
-Event Information
-Flash ADC Data (optional)
-ATWD Channel 0 Data (optional)
-ATWD Channel 1 Data (optional)
-ATWD Channel 2 Data (optional)
-ATWD Channel 3 Data (optional)

The order in which these blocks appear is fixed and the presence or absence of any of the optional blocks can be inferred from fields contained in the event header. When mapping these fields onto memory locations, it should be noted that while the "Endian-ness" of multibyte quantities contained within this format are consistent for an entire event, they can vary from one data source to another. For example, data from a simulation program may be little endian while that generated by the DOM FPGA may be little endian. In all cases, the "endian-ness" of an event can be determined by examining the event format identifier found in the event header. This value has been promoted to a 16-bit value in order to allow unambiguous determination of the byte ordering found throughout the event. Thus when this field, read as a 16-bit quantity, gives a value of 0x0001 the event is written as a little-endian structure. When this field read as 0x0100, the event has been formatted as a big-endian structure. Detailed contents of each block follow.

Format IDs:

Currently two formats exist, labeled "1" and "2". Format 1 has been in use throughout the FAT cycles of 2004. Format 2 is identical to format 1, with the inclusion of extra bits in the event trigger flag (see **Trigger Flags**, below; changes specific to Format 2 are in ***bold italics***).

Event Header:
This block contains fields that describe the length and format type of the event that follows. It contains additional fixed-length fields that help in de-blocking data that may appear later within this event.

Quantity	Datum Size	Length	Comments
Event length	Short (16 bits)	Single value	Length of event in bytes
Event format ID	Short (16 bits)	Single value	Value, corrected for "endian ness" is 1 or 2
Miscellaneous	Byte	One value	See following table.
Number of Flash ADC samples	Byte	One value	See Flash ADC Data section below.
ATWD0 & 1 format flag	Byte	One value	Two 4-bit fields that describe appearance of data from ATWD 0 & 1. Value=ATWD1desc<<4+ATWD0 desc. See ATWD Data section below.
ATWD2 & 3 format flag	Byte	One value	Two 4-bit fields that describe appearance of data from ATWD 2 & 3. Value=ATWD3desc<<4+ATWD2 desc. See ATWD Data section below.

Bit values for miscellaneous field

Quantity	**Datum Size**	**Length**	**Comments**
ATWD used in readout	One bit	One bit	Value of 0 indicates ATWD 0, 1 indicates ATWD1
TBD			

Format for ATWD format flags

Description	Bit 3	Bit 2	Bit 1	Bit 0
ATWD not present	X	X	X	0
Byte data, 32 samples	0	0	0	1
Byte data, 64 samples	0	1	0	1
Byte data, 16 samples	1	0	0	1
Byte data, 128 samples	1	1	0	1
Short data, 32 samples	0	0	1	1
Short data, 64 samples	0	1	1	1
Short data, 16 samples	1	0	1	1
Short data, 128 samples	1	1	1	1

Event Information:
This block contains trigger and time stamp information for this event.

Quantity	Datum Size	Length	Comments
Event trigger flag	Byte	One value.	Bit mapped trigger descriptor. See following table for values.
Spare	Byte	One value	Future use and to promote byte alignment.
Time stamp	48 bits (6 bytes)	One value	Non-standard length type. "Endian-ness" matches rest of event.

Trigger Flags:
Bits 1..0 represent the trigger type;
"Status" bits 7..3 signal special circumstances, as follows:

Trigger (Bits 1..0)	**Value**	**Comments**
Test pattern trigger	0x0	
CPU requested trigger	0x1	
SPE discriminator trigger	0x2	
Flasher board trigger	0x3	**ATWD reads out flasher board trigger**
Bit 2		**Reserved**
Status (Bits 7..3)	**Name/Meaning**	**Comments**
Bit 7	UNKNOWN_MODE	In case of an invalid trigger setting, the UNKNOWN_MODE is set and the test pattern trigger is used
Bit 6 (Format 2 only!)	***LC_UPPER***	***Set if local coincidence requirement is met, and LC has been configured to be received by the upper DOM***
Bit 5 (Format 2 only!)	***LC_LOWER***	***Same as bit 6 but for lower DOM***
Bit 4 (Format 2 only!)	***FB_RUN***	***Set if flasher board run is in progress (ATWD waveforms are then digitization of LED current.***
Bit 3 (Format 2 only!)	***LC_REQUIRE_BOTH***	***This is set if signals from both upper and lower DOMs are required to satisfy local coincidence***

Format 2 only: Please note that in testdomapp, in the current FPGA implementation, there is no information available that would indicate which neighboring DOM (upper or lower) caused the LC condition to be met; rather, bits 5 and 6 are a reflection of how the DOM was configured at the time of the event. So if LC receive is enabled for both upper and lower DOMs, both bits 5 and 6 will be set in the event record.

Flash ADC Data:
This block will contain a variable length set of 16 bit samples from the flash ADC. The number of samples appearing can be determined by examination of the appropriate field

in the event header block. Unlike data from the ATWD, all time samples, regardless of number, will appear in correct, increasing time sequence.

Quantity	Datum Size	Length
Flash ADC data	Short (16 bits)	0 to 255 samples as indicated in event header block

---

ATWD Channel 0 Data:
Block will contain data as described by one of the rows of the following table based on value of ATWD format flag found in appropriate field within the event header block.

Quantity	ATWD format flag **	Datum Size	Length
ATWD channel 0 data	0x1	Byte	32 samples *
ATWD channel 0 data	0x5	Byte	64 samples *
ATWD channel 0 data	0x9	Byte	16 samples *
ATWD channel 0 data	0xd	Byte	128 samples *
ATWD channel 0 data	0x3	Short (16 bit)	32 samples *
ATWD channel 0 data	0x7	Short (16 bit)	64 samples *
ATWD channel 0 data	0xb	Short (16 bit)	16 samples *
ATWD channel 0 data	0xf	Short (16 bits)	128 samples *

- * Note that all samples are readout in reverse time order. That is, last time sample value appears first.
- ** Note that any value with lsb=0 (e.g. 0, 2, 4..) indicates no data present for this ATWD channel.

ATWD Channel 1 Data:
Block will contain data as described by one of the rows of the following table based on value of ATWD format flag found in appropriate field within the event header block.

Quantity	ATWD format flag **	Datum Size	Length
ATWD channel 1 data	0x1	Byte	32 samples *
ATWD channel 1 data	0x5	Byte	64 samples *
ATWD channel 1 data	0x9	Byte	16 samples *
ATWD channel 1 data	0xd	Byte	128 samples *
ATWD channel 1 data	0x3	Short (16 bit)	32 samples *
ATWD channel 1 data	0x7	Short (16 bit)	64 samples *
ATWD channel 1 data	0xb	Short (16 bit)	16 samples *
ATWD channel 1 data	0xf	Short (16 bits)	128 samples *

- * Note that all samples are readout in reverse time order. That is, last time sample value appears first.
- ** Note that any value with lsb=0 (e.g. 0, 2, 4..) indicates no data present for this ATWD channel.

ATWD Channel 2 Data:
Block will contain data as described by one of the rows of the following table based on value of ATWD format flag found in appropriate field within the event header block.

Quantity	ATWD format flag **	Datum Size	Length
ATWD channel 2 data	0x1	Byte	32 samples *
ATWD channel 2 data	0x5	Byte	64 samples *
ATWD channel 2 data	0x9	Byte	16 samples *
ATWD channel 2 data	0xd	Byte	128 samples *
ATWD channel 2 data	0x3	Short (16 bit)	32 samples *
ATWD channel 2 data	0x7	Short (16 bit)	64 samples *

ATWD channel 2 data	0xb	Short (16 bit)	16 samples *
ATWD channel 2 data	0xf	Short (16 bits)	128 samples *

- * Note that all samples are readout in reverse time order. That is, last time sample value appears first.
- ** Note that any value with lsb=0 (e.g. 0, 2, 4..) indicates no data present for this ATWD channel.

ATWD Channel 3 Data:
Block will contain data as described by one of the rows of the following table based on value of ATWD format flag found in appropriate field within the event header block.

Quantity	**ATWD format flag ****	**Datum Size**	**Length**
ATWD channel 3 data	0x1	Byte	32 samples *
ATWD channel 3 data	0x5	Byte	64 samples *
ATWD channel 3 data	0x9	Byte	16 samples *
ATWD channel 3 data	0xd	Byte	128 samples *
ATWD channel 3 data	0x3	Short (16 bit)	32 samples *
ATWD channel 3 data	0x7	Short (16 bit)	64 samples *
ATWD channel 3 data	0xb	Short (16 bit)	16 samples *
ATWD channel 3 data	0xf	Short (16 bits)	128 samples *

- * Note that all samples are readout in reverse time order. That is, last time sample value appears first.
- ** Note that any value with lsb=0 (e.g. 0, 2, 4..) indicates no data present for this ATWD channel.

Modification History

V1.1 1/19/2004 JEJ Changed 96 sample option to 16 samples to support forthcoming tests at PSL.

V1.2 3/16/04 DEH Updated the event trigger byte value table to match changes made to the DOM Application.

V1.3 12/02/04 JEJ – added definition for format 2 with LC enable bits added.

V1.4 12/09/04 JEJ – added FB run bit to format 2 trigger flags
V1.5 02/01/05 JEJ – added trigger type 3 (flasher board LED current trigger)
V1.6 10/20/05 JEJ – added extra bit to show requirement of “up AND down” for LC