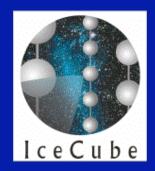


IceCube DOM Development

John Kelley October 1, 2003



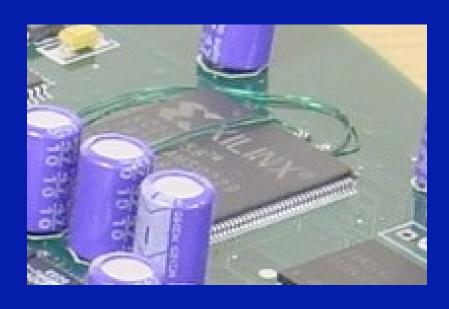
- DOM Mainboard Overview
- STF Test Development
- ATWD Ping-Pong Mode
- IceTop Second Penetrator

Mainboard Overview



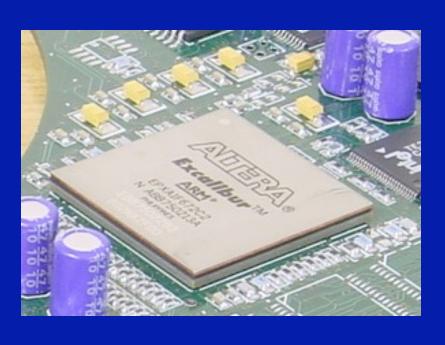
- ARM microprocessor
- Programmable devices: FPGA, CPLD, serial PROM
- Flash memory file system

Xilinx CPLD



- CPLD = complex programmable logic device
- Firmware in VHDL
- Lower-level functions: HV, Flasherboard interfaces
- Stores firmware w/o power, but harder to change (JTAG)

Excalibur: FPGA+ARM



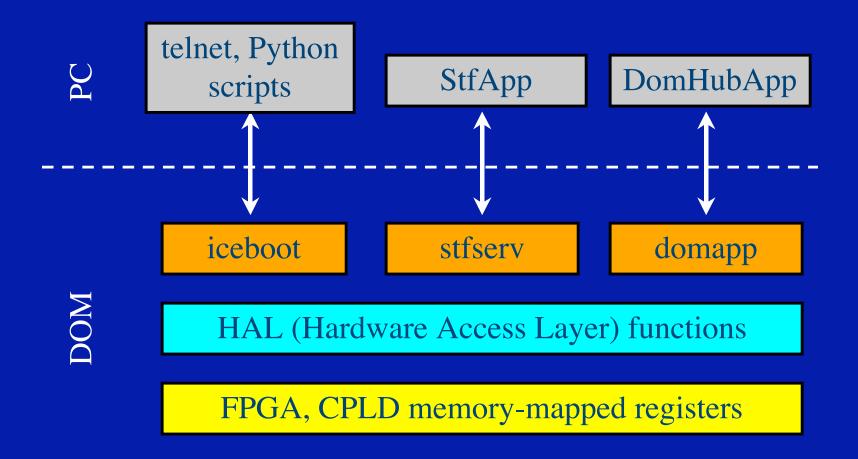
- FPGA = field programmable gate array
- Firmware in VHDL (mostly)
- Controls triggers, communications, etc.
- Must reload after powercycle, but easy to do
- EPXA1 vs. EPXA4

Excalibur: FPGA+ARM



- ARM9 processor core
- High-level MB software (iceboot, domapp, stfserv)
- Most software in C; crosscompiled on Linux and then downloaded to flash file system

DOM Software Structure



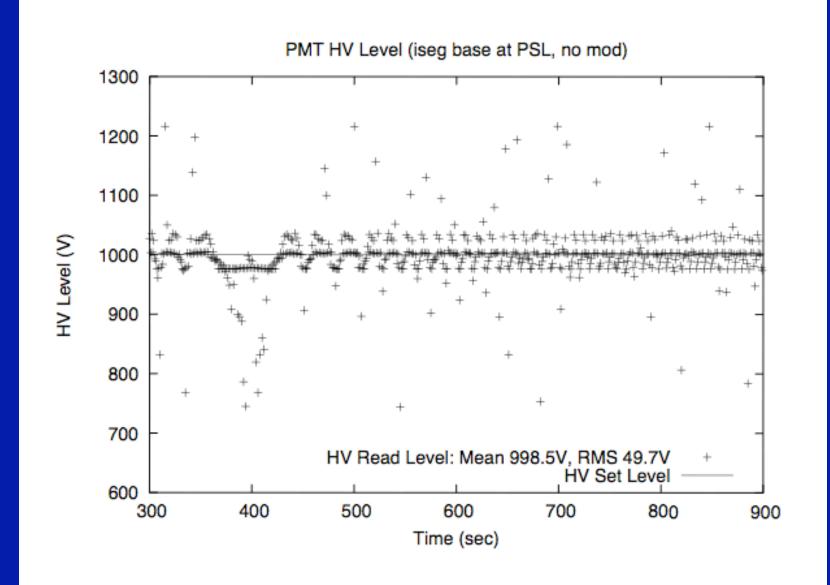
STF: Standard Test Framework

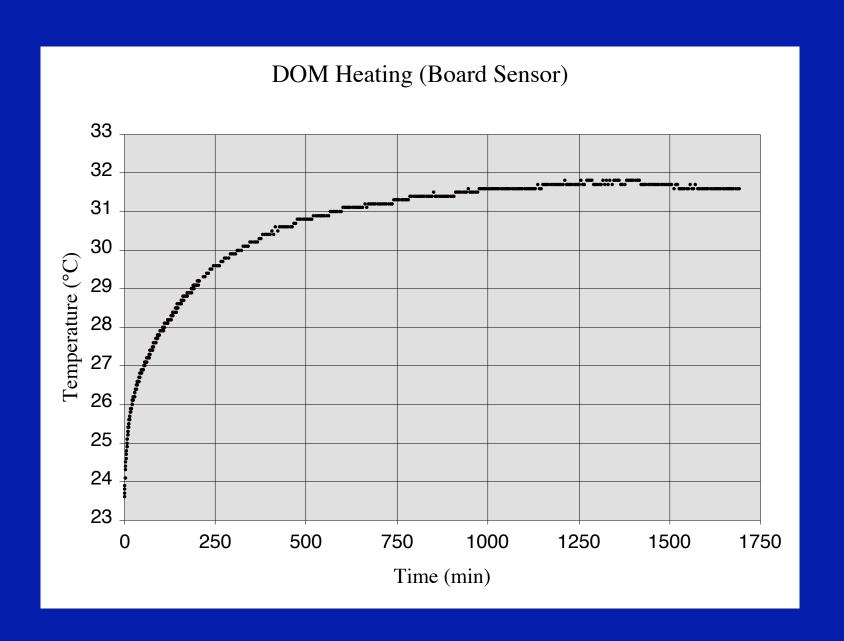
High Voltage Stability

High Voltage Ramp

• Self-Heating (ad hoc)

• PMT P/V Ratio (in progress)





ATWD Ping-Pong Mode

- ATWD: Analog Transient Waveform Digitizer
- Digitizes PMT pulses
- Largely controlled by FPGA

ATWD Ping-Pong Mode

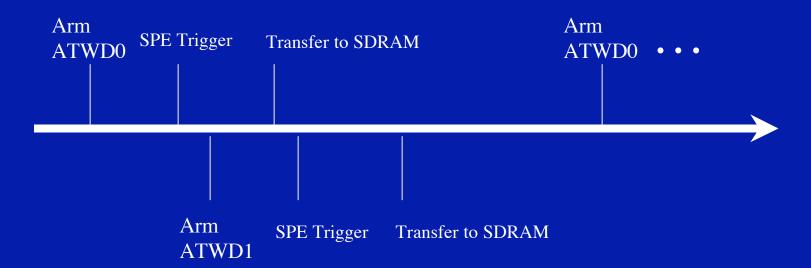
- ATWD: Analog Transient Waveform Digitizer
- Digitizes PMT pulses
- Largely controlled by FPGA



Without Ping-Pong:



With Ping-Pong:



Gory Implementation Details

- FPGA firmware modified for new ATWD trigger control (two interlocked state machines); also added timestamping
- ATWD readout handshaking (SDRAM transfer still controlled by software)
- Ping-pong HAL calls
- Packaged in an iceboot function, "acq-pp"
- Improves maximum acquisition rate (burst) to ~10 kHz

IceTop Penetrator

- Serial PROM will contain (changing) comm. protocol code (configboot)
- Expose JTAG port via buffer circuitry, 2nd penetrator, serial cable

