# A Status of the PMm$^2$ Project

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on behalf of the PMm$^2$ collaboration

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University of Hawaii, Manoa
August 13–15, 2009




ULB UNIVERSITÉ LIBRE DE BRUXELLES, UNIVERSITÉ D'EUROPE

# Scope of Project

- Develop ASIC for high-density, low-power readout of huge array of PMT. New megaton $H_2O$ or liquid scintillator detectors will require $O(10^5)$ photomultiplier channels.
  - Physics channels are proton decay, LBL neutrino oscillations, neutrino astrophysics (ATMNU, supernovae)
  - Desired coverage: ≈ 40%
  - Two approaches
    - Increase active photodetector area: Super-K approach - need about 40,000 20″ PMTs. Advantage is reduced channel density.
    - Smaller 12″ PMTs cheaper, more easily manufacturable and allow higher pixel density but need 2.5 × number of DAQ channels.
- Proof-of-concept of local in-water electronics - PMT anode signal path ~ 1 m. Reduce count of ~100 m cables to surface DAQ. Hi-rel electronics, water-tight enclosure*.
- Develop with Photonis 12″ pressure-resistant PMT suitable for single-photon detection.
- Deliver demonstrator module that integrates these ideas and test electronics
- Separate, but related MEMPHYNO project to prove concept using next-higher level of integration (full H2O tank with muon hodo to study basic physics capability).

* Electronics could also be located entirely at surface.

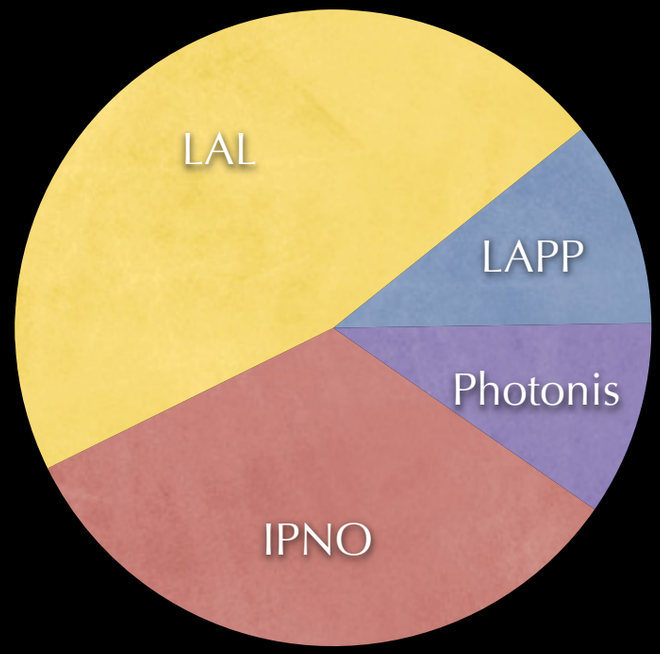
# PMm² Project (2007–2010)

- **LAL Orsay**
  - front-end electronics
  - water-tight box
- **IPN Orsay**
  - photodetector tests
  - mechanical structure
  - board-level integration
- **LAPP**
  - DAQ readout electronics
  - Cables
- **Photonis**

  PMT supplier - departed March 2009 due to cessation of PMT activity.

- **ULB (02/2009+)**

  Data acquisition software (TCP DAQ client)




~500 k€ funding over 3 years to support 5 FTE engineers and 1 postdoc. Approx 20 people on project

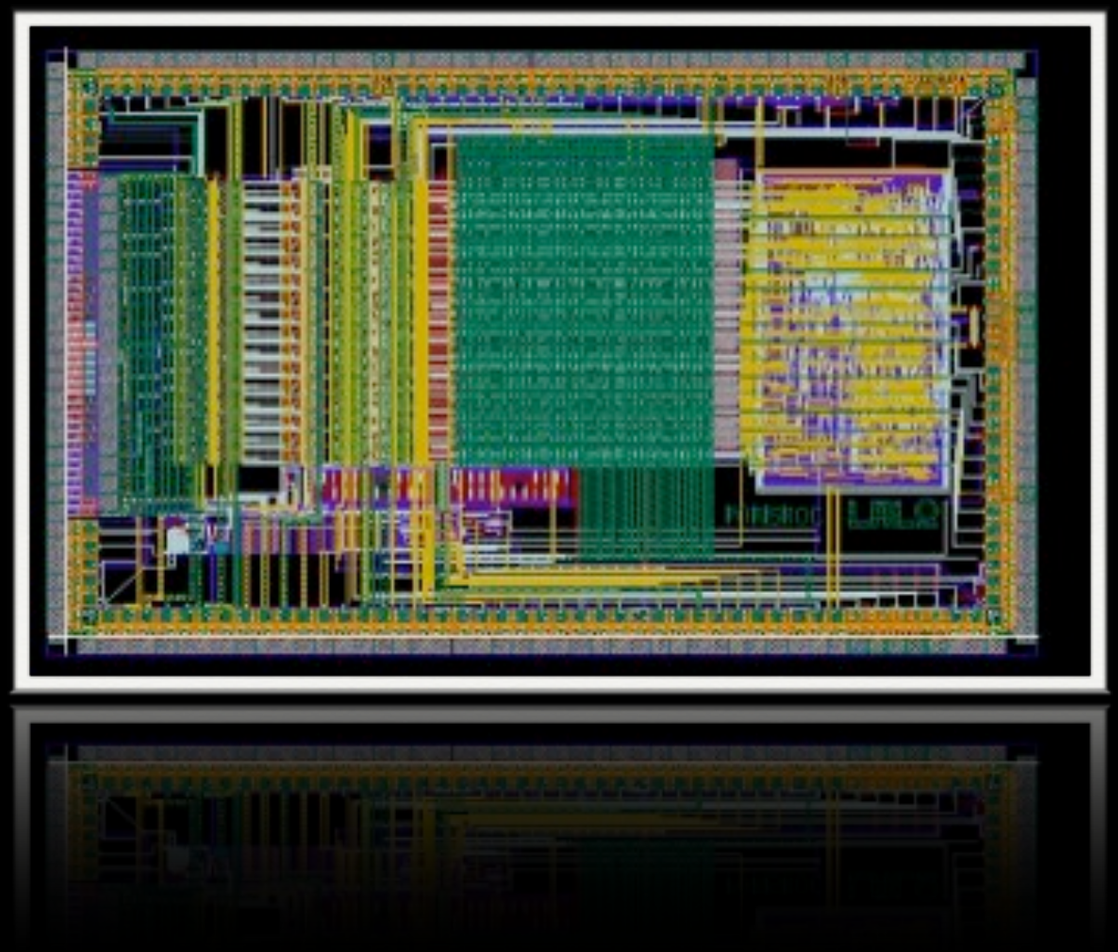
# PARISROC

Photomultipler array integrated in SiGe readout chip

An OMEGA product

Orsay MicroElectronics Group Associated

ASIC based on 0.35µm AMS SiGe process
Die size 5 mm × 3.4 mm
Package 160-pin CQFP

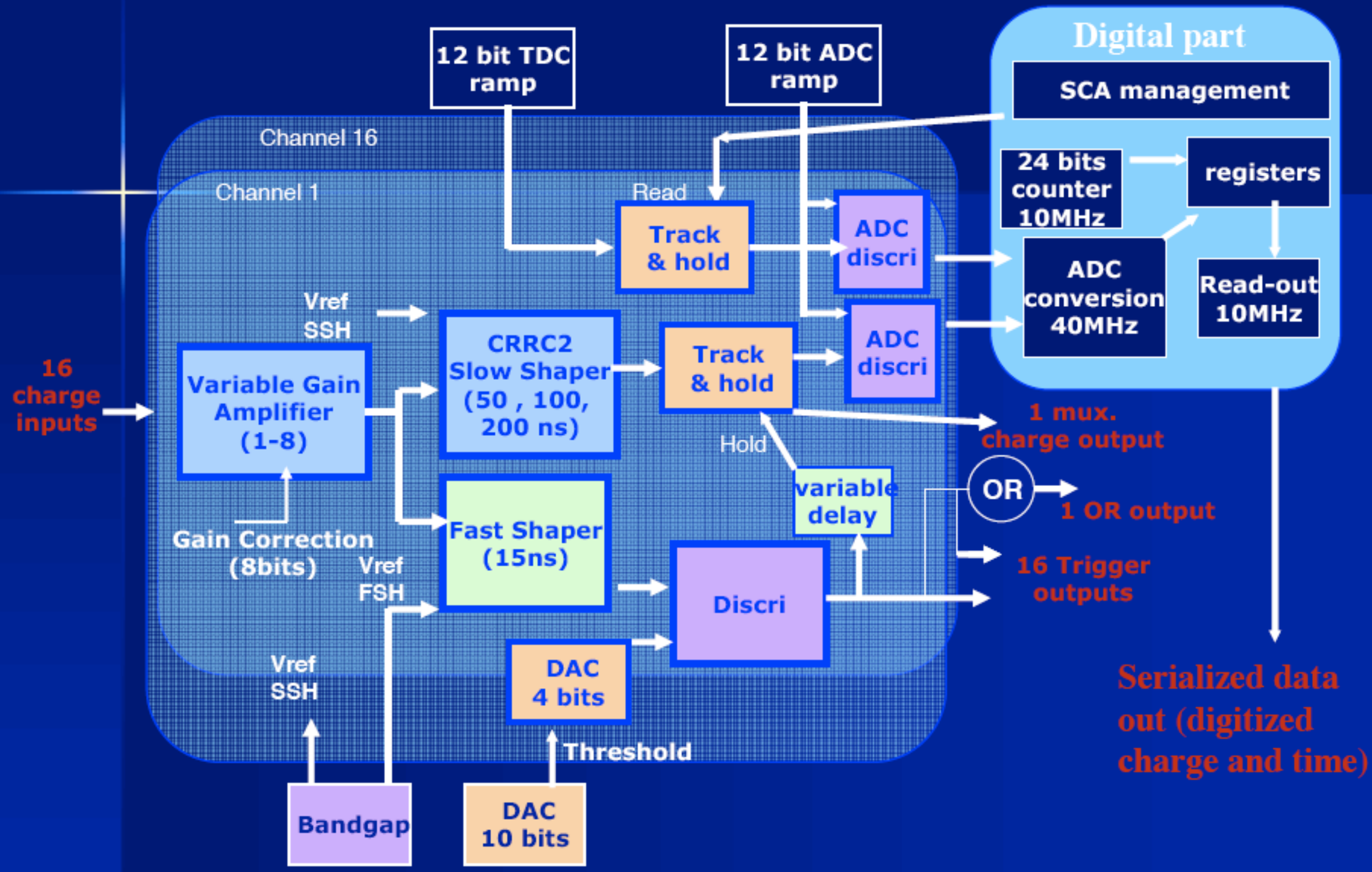


# PARISROC

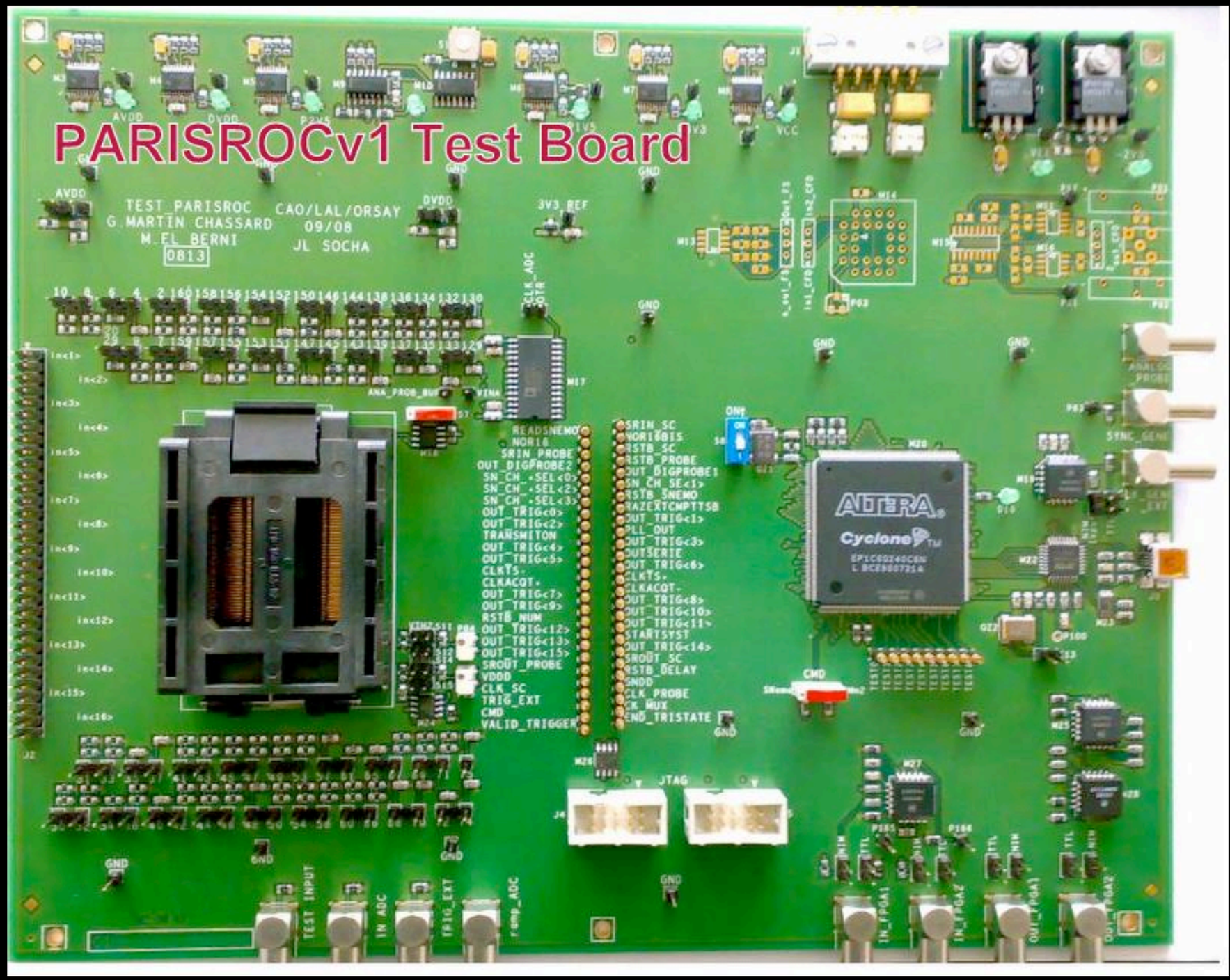
- 16 x PMT inputs
  - Time stamping to < 1 ns resolution
  - Pulse charge integration dynamic range 0 - 300 pe
- Each channel has variable gain to compensate for gain-vs-HV manufacturing spread (only 1 HV generator per 16 PMT)
- Digitization on-chip - 10-bit ADC/TDC
- Triggerless - all hits passing PMT anode signal discriminator will appear in digital data stream.
- Low power ~20 mW / channel
- Low cost - 10 € / chip

# PArISROC v1 architecture

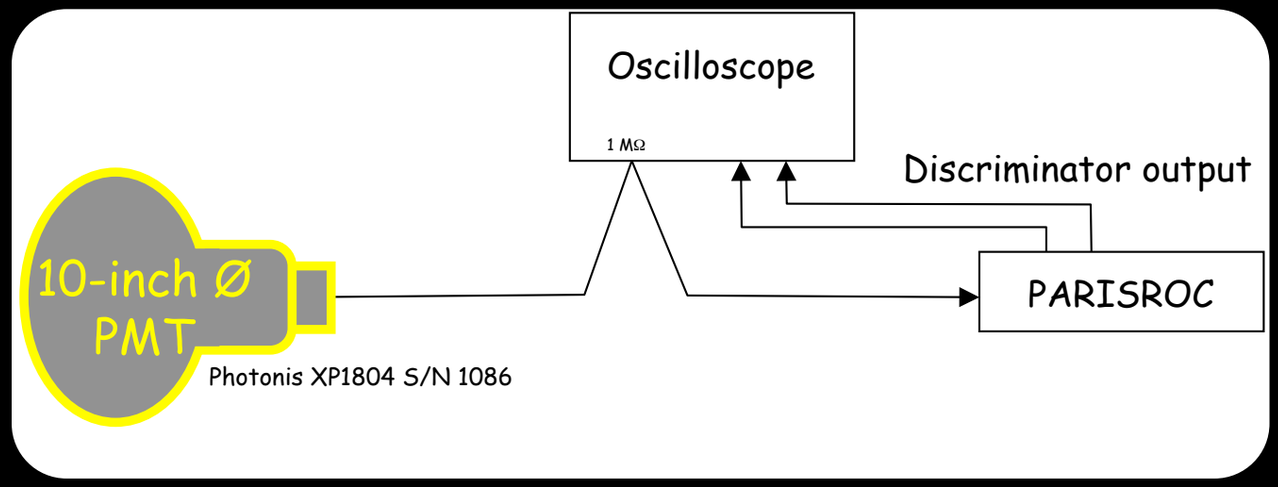
LAL



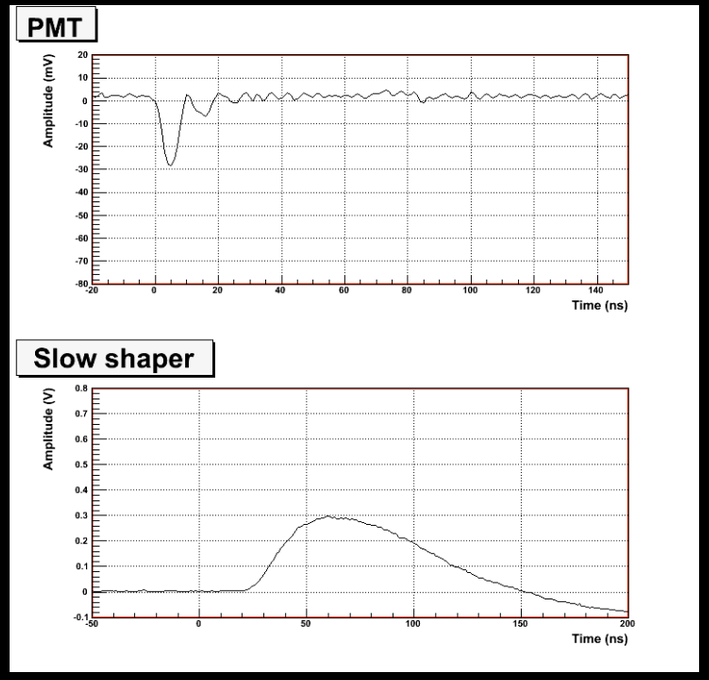
# PARISROC Test Board



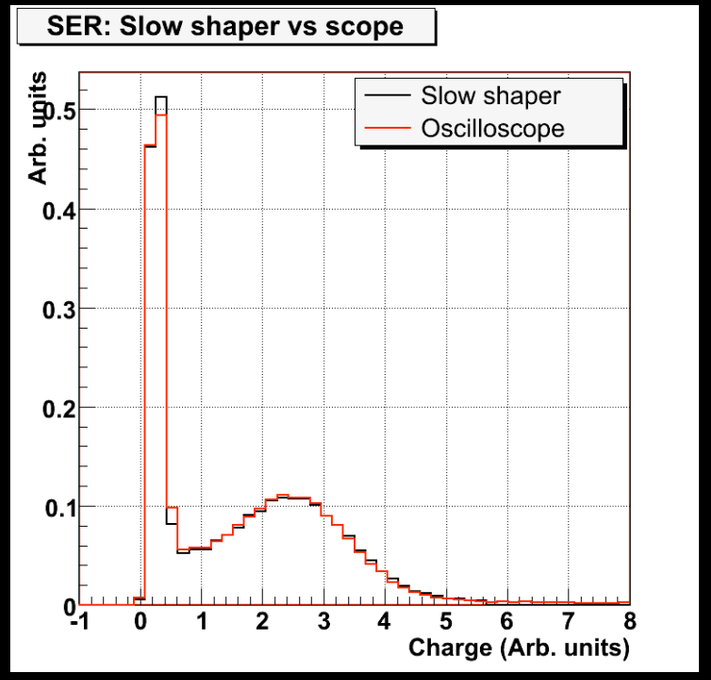
# Tests of PARISROC w 10″ PMT



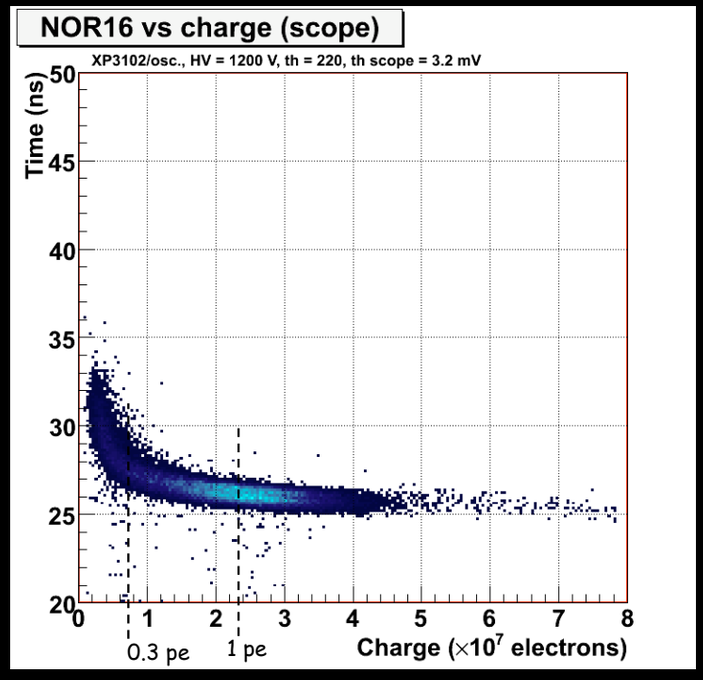

Tests / graphics by B. Geniolini (IPNO)




Transient response of slow shaper compared to anode current pulse observed by DSO.




SPE repsonse comparing output of slow shaper to DSO at 2.4E7 gain.




Time resolution measurements taken with XP3102 1″ PMT comparing $T_{NOR16}$ - $T_{PMT,DSO}$. At 0.3 pe discriminator threshold the RMS width is 660 ps.

# PARISROC v2

- 2nd rev of ASIC planned for production late 2009
- Addresses some minor bugs with v1 of chip (actually v1 worked remarkably well) - bugs include total loss of one channel due to design error not caught until after artwork submitted to foundry; increase noise level.
- Improvements / new features
  - 2 gains for charge measurement
  - ADC resolution decreased from 12 to 10 bits to reduce deadtime from 1% to approx 0.25% (assuming 5 kHz singles rate).
  - Improvements to reduce coarse and fine time stamping jitter
  - Increase clock to 40 MHz to further reduce readout time by 4×.
- Possibility time / money for Rev 3 to correct bugs in v2.

# PARISROC v2 LAL

2 gains per channel
0-10pe & 0-300pe
8-9-10 bits ADC/TDC

Ramp TDC
SCA fine time
Time output
Ramp ADC
Charge output
PA
SSH
SCA low gain
MUX
SSH
SCA high gain
50 Ω
ext
ext. Hold
OR
Hold
VARIABLE DELAY
Auto-trig
Threshold
gain Output
PA
FSH
Discri.
Adjustable gain amplifier
Adjust = 1-4
4-bit DAC
Threshold
Trigger Output
Ramp TDC, Ramp ADC and 10-bit DAC common to all channels
10-bit DAC
10-bit DAC
10-bit DAC
Added blocs

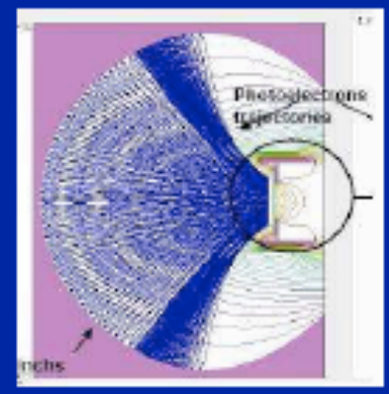
# Photodetector




IPNO shape and glass thickness computation to subtend 10 bars

Photonis Electrostatic and realisation of 9 pieces (Sept. 08)





First measurements:

- Photocathode:
  - uniformity quite good
  - Skcb=10.5$\mu$A/lmF (with corning blue filter)
  - Skb=77$\mu$A/lm (with white source)
  - ~24% at peak => reasonable for first attempt

  (nb: 8" XP1886 new process bialkali super² gives 36% at peak)
- Gain:
  - $10^5$ @ 2kV => low value compared to expectation $10^6$ (8 stages)
  - Redesign of the first dynode

Potting tested



PHOTONIS had halt the PM activity March 09

IPNO

# Implosion simulation

12”:31cm

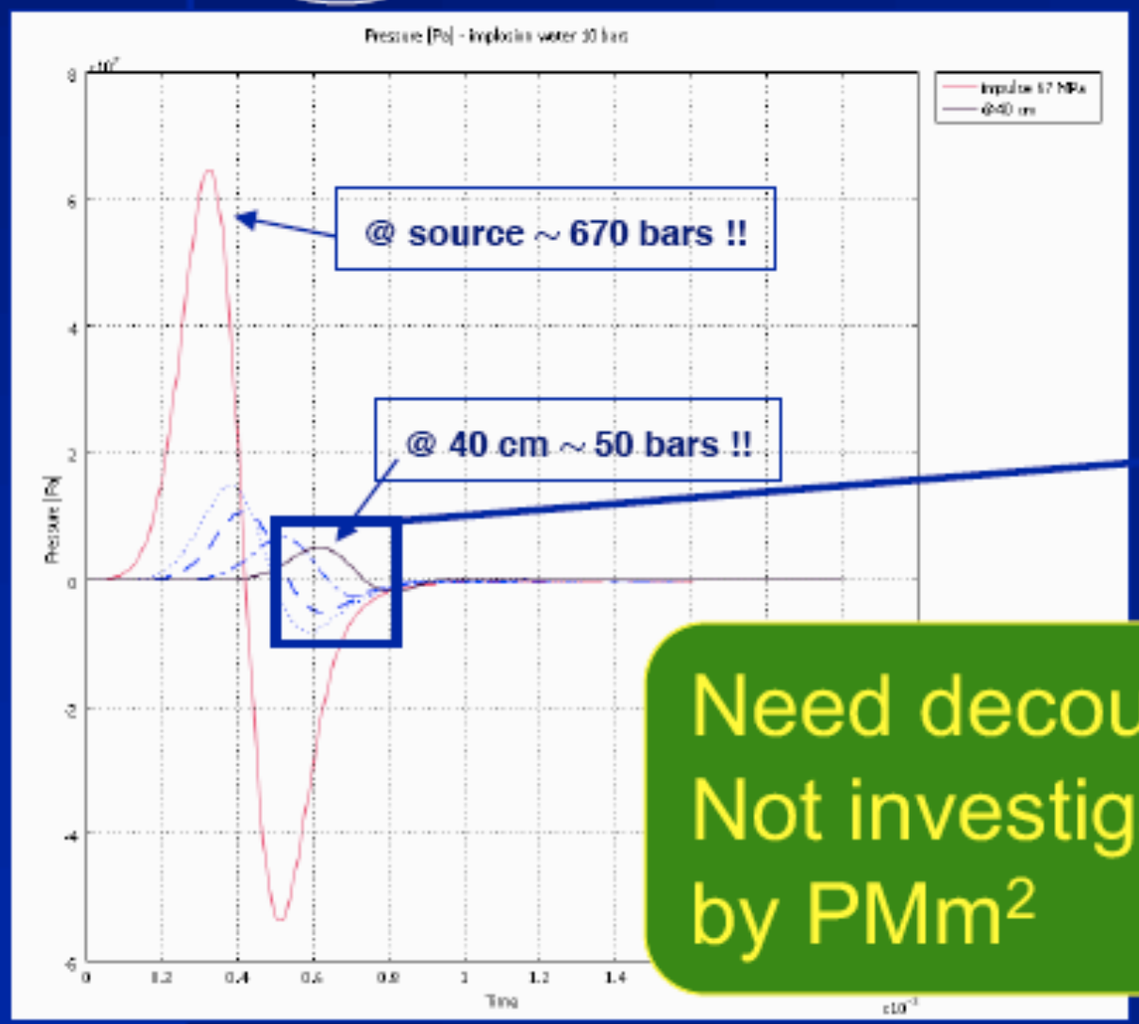
47,5cm

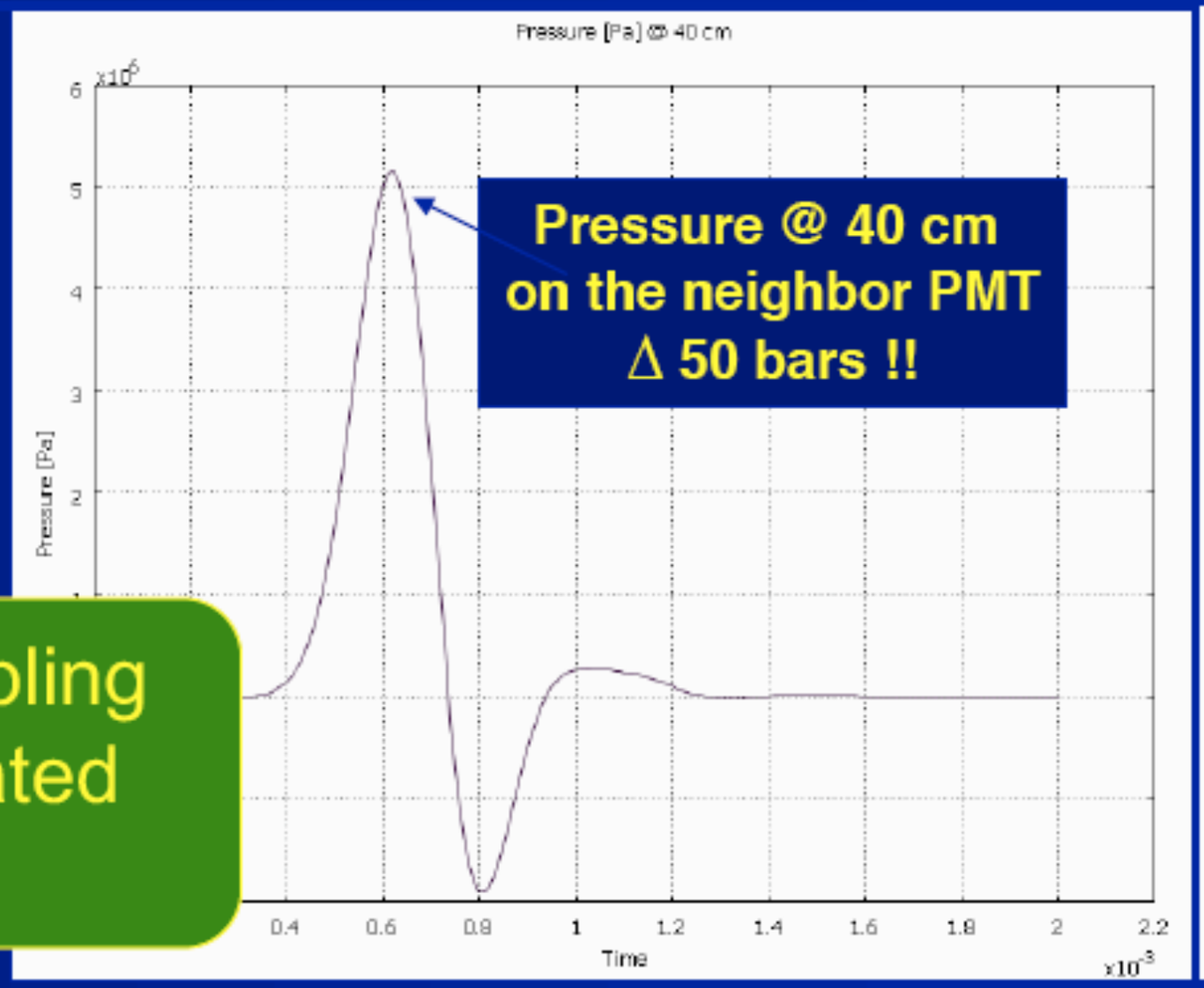
CONSOL software

+

Semi-analytical approach

Preliminary validated with exp. data




Need decoupling
Not investigated
by PMm²

IPNO

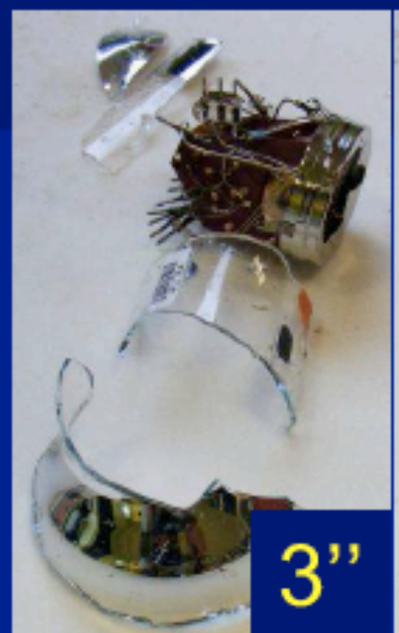
# High pressure tests

BNL tank (150b)



Mid-Feb 09



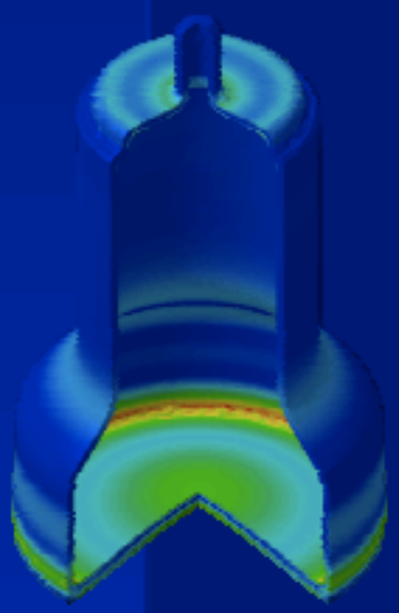









3,2 atm 6,5 atm 16,3 atm



Preliminary comparison simulation/measurements indicates

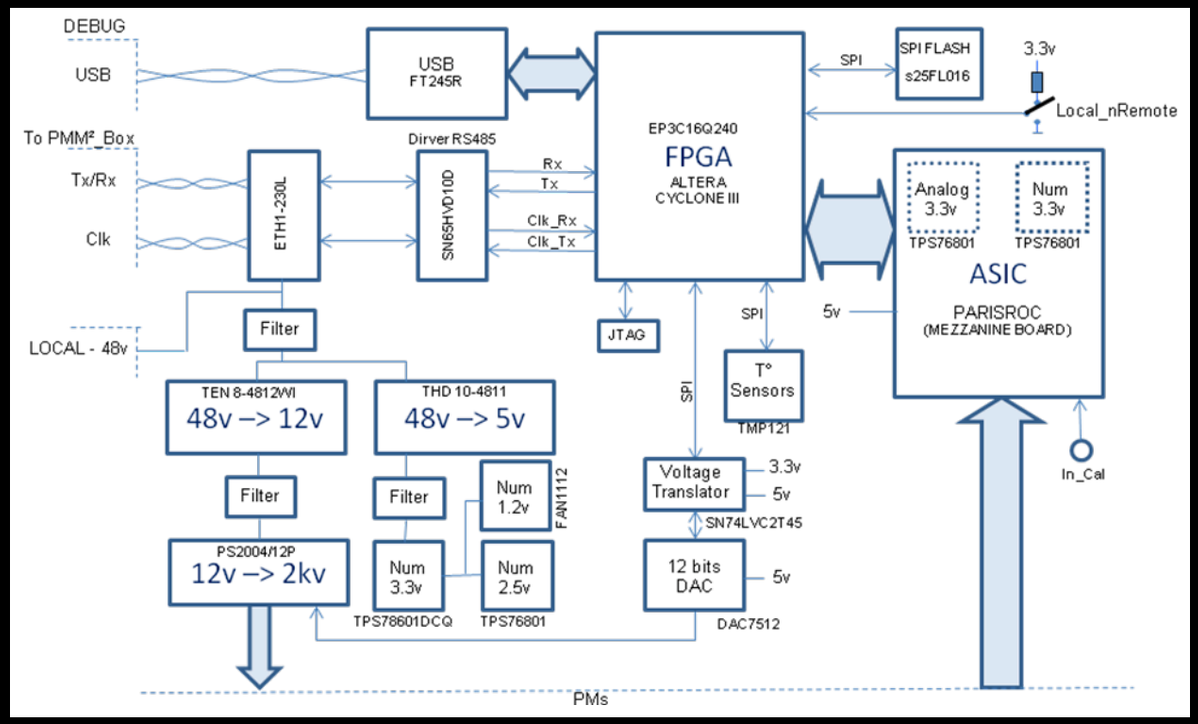
**Beaking limit of glass : 40 - 50 MPa**

In agreement with glass properties given by Manufacturer. This is a good news **to design a 12'' shape and choose glass thickness to subtend 10 atm.** **(first test with 12'' end march 09')**

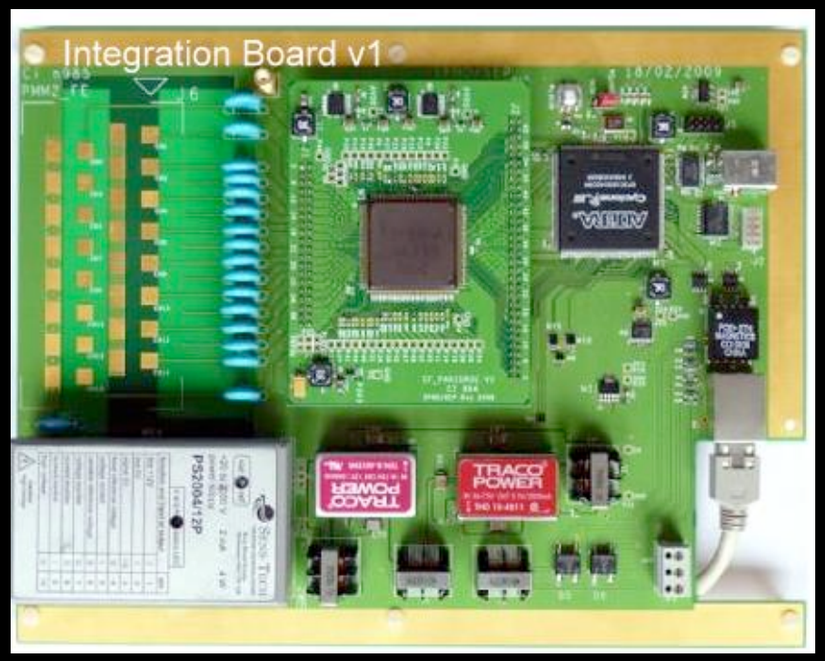
8'' **XP18060** for Daya Bay (reinforced) does **not break at 10 atm**

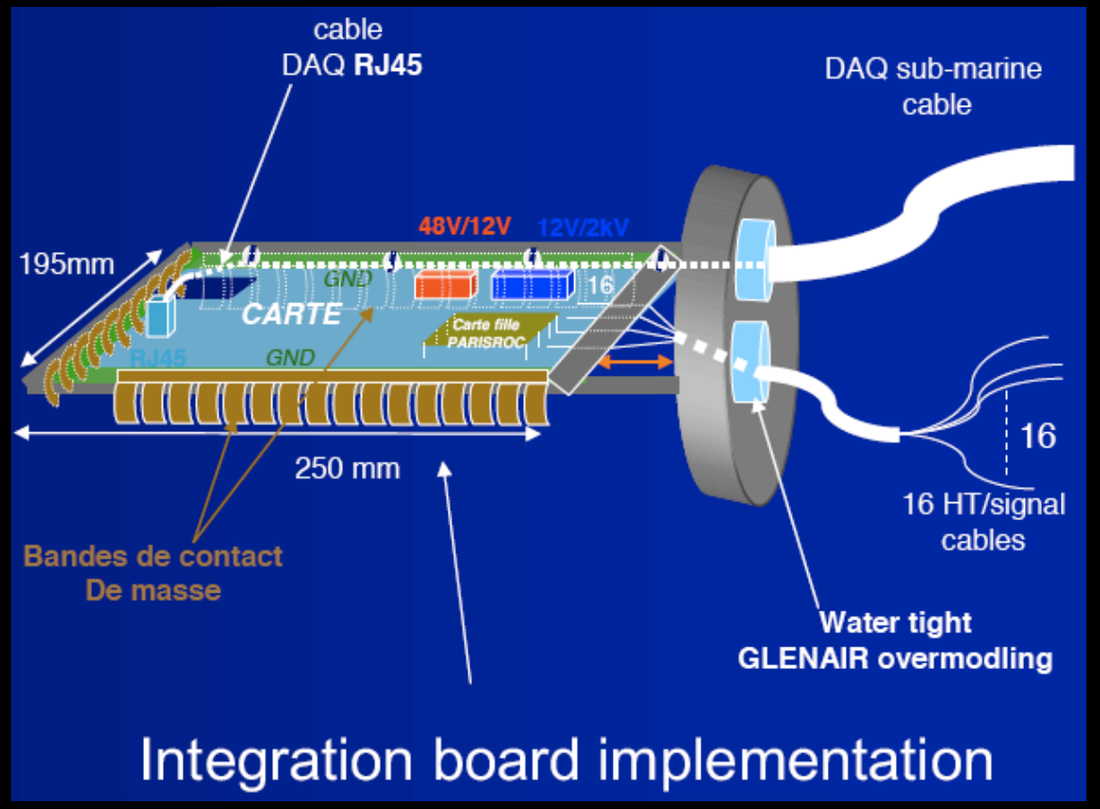
J.E Campagne Omega Users 2/07/2009

# Integration Board

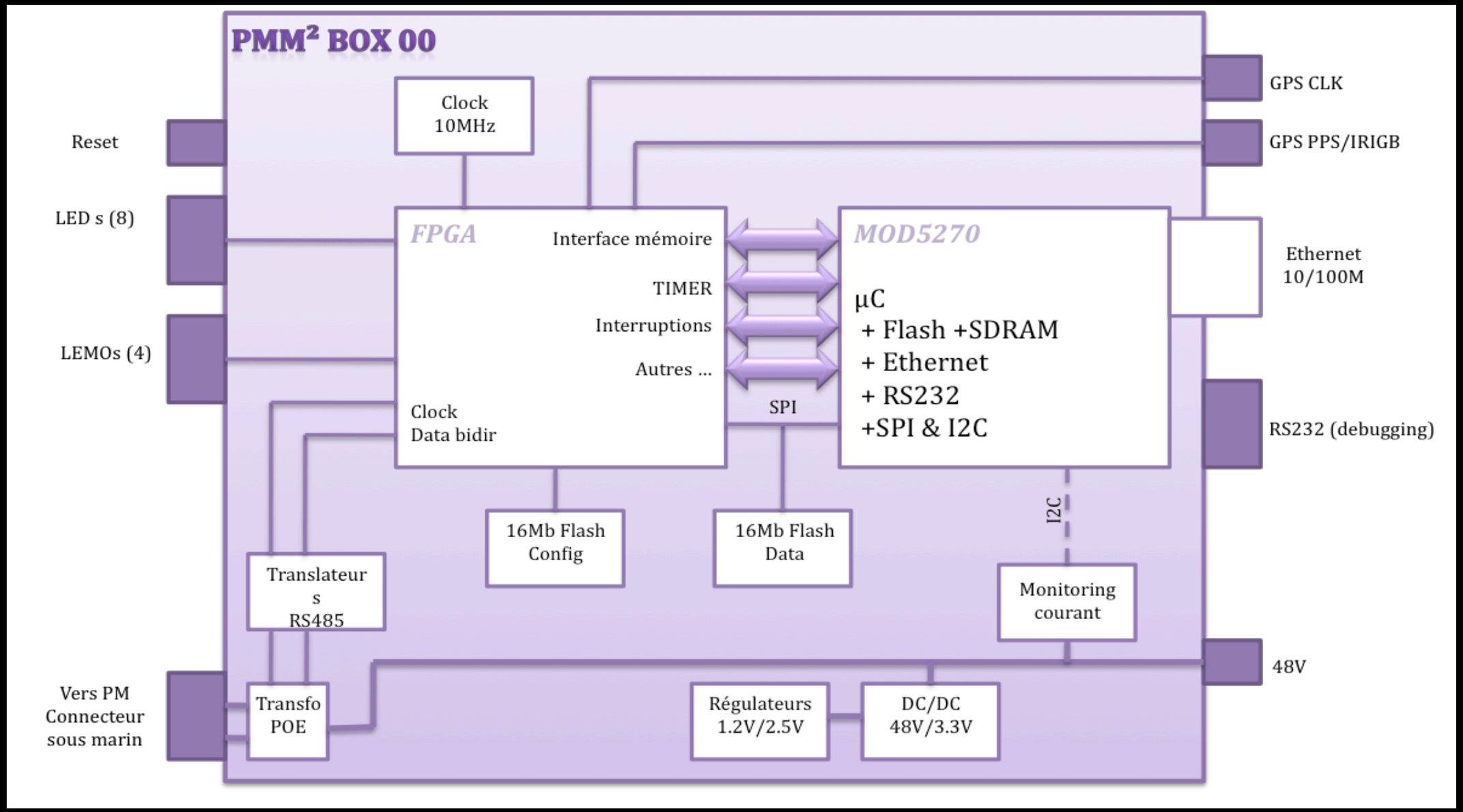




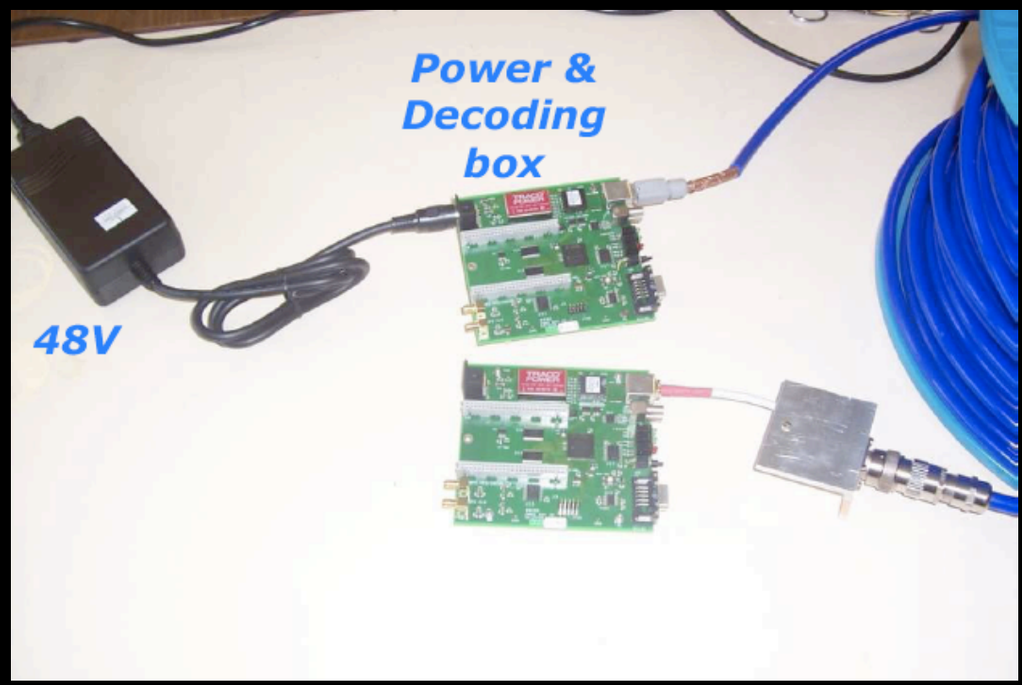



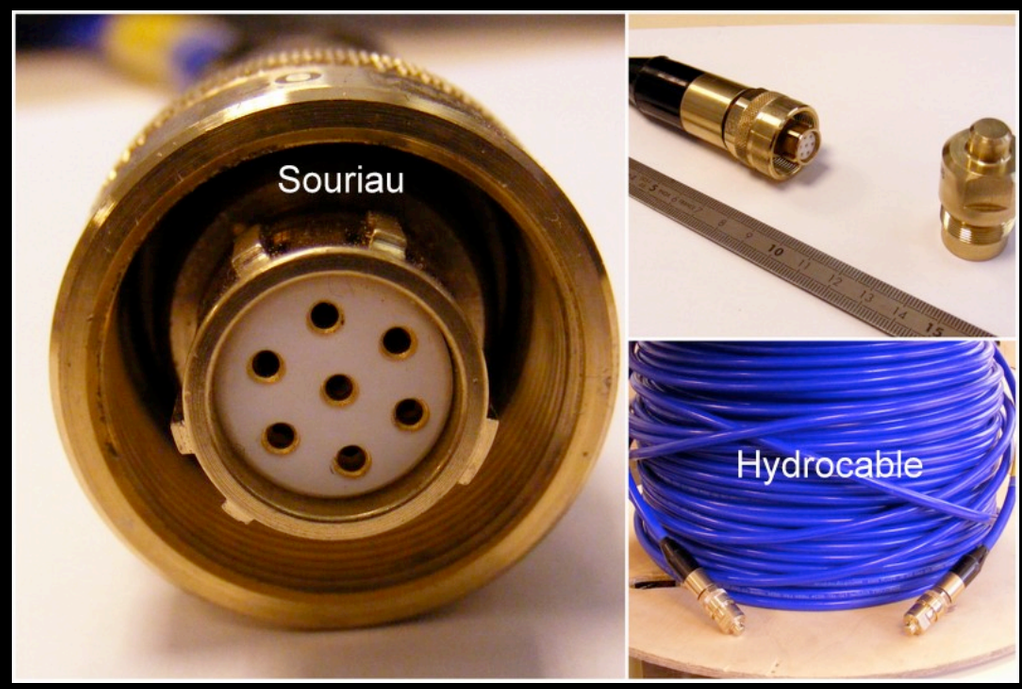
# Power & Decoding Board



# Communications Tests (LAPP)

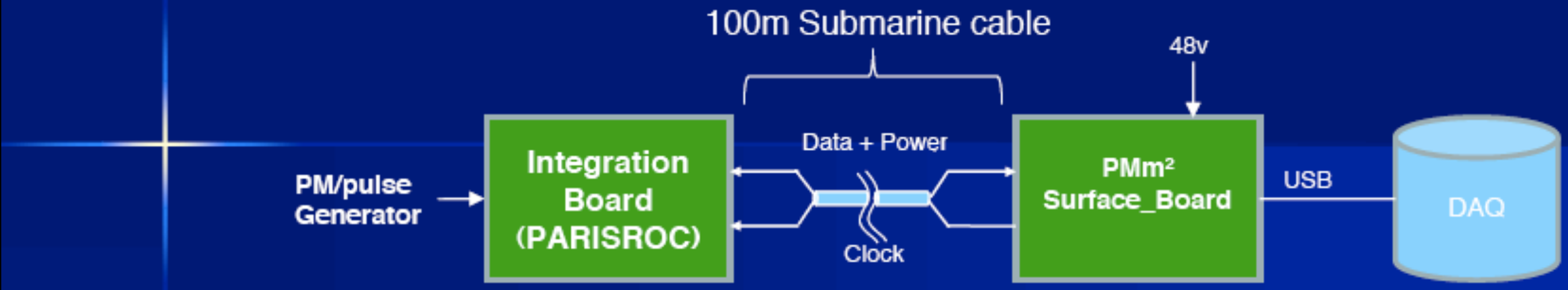
- Throughput over 100 m communication cable tested by LAPP
- With random bit patterns of 512 b data blocks 3h tests conducted in April
  - 8.5 Mbps sustained data rate
  - No errors detected ($BER_{90} < 2.6 \times 10^{-11}$)



# PMm² DAQ tests

IPNO+LAPP+LAL



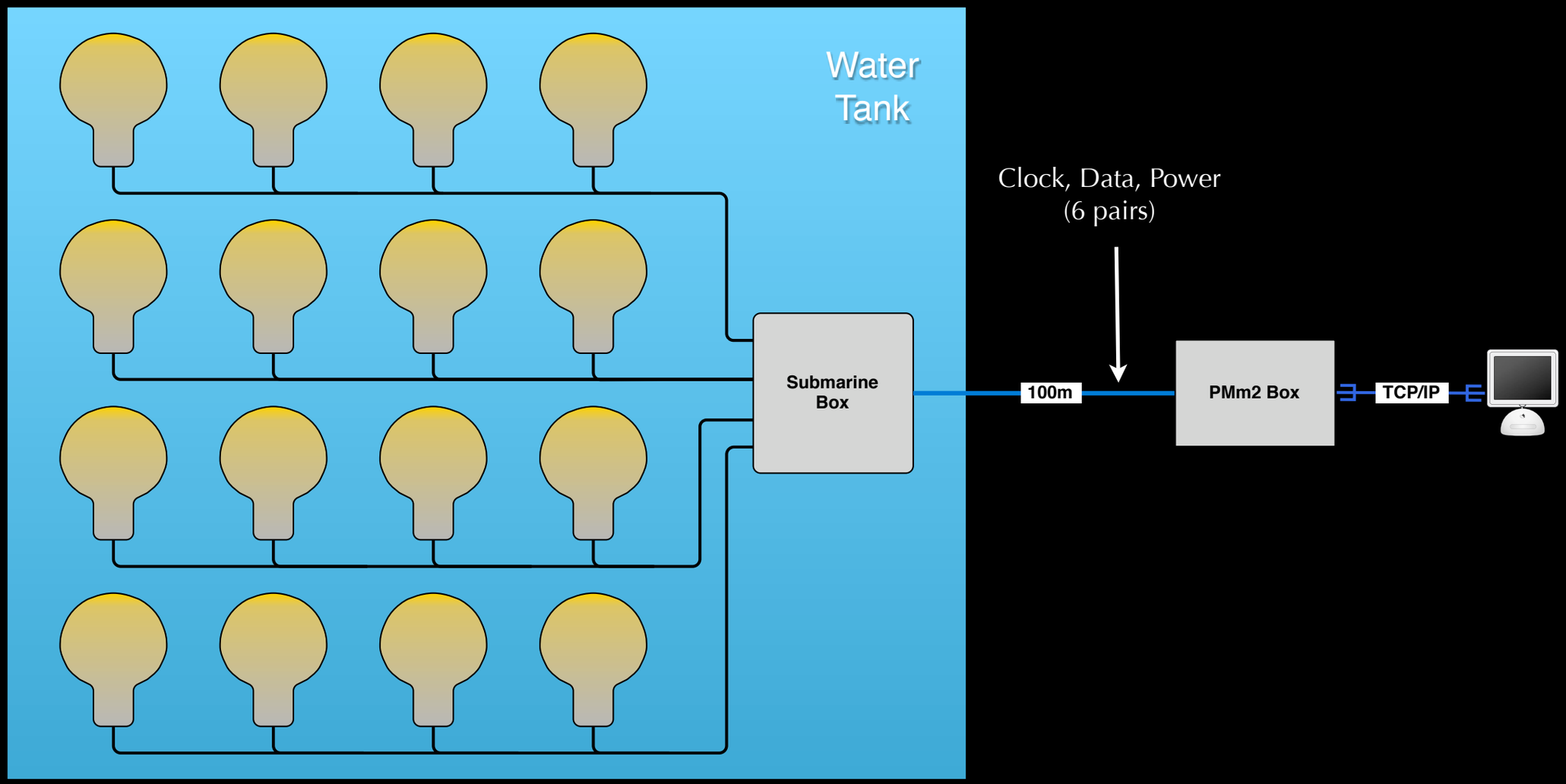



Injection up to 16 channels ( test input)
Pulse period 200$\mu s$

Transmission tests during several hours
Ok for 1 complet set.

Next steps:
1) Use 1 PMs as « noise pulser »
2) Use several PMs
3) Use the TCP/IP network for the DAQ
4) …

# Demonstrator Schematic



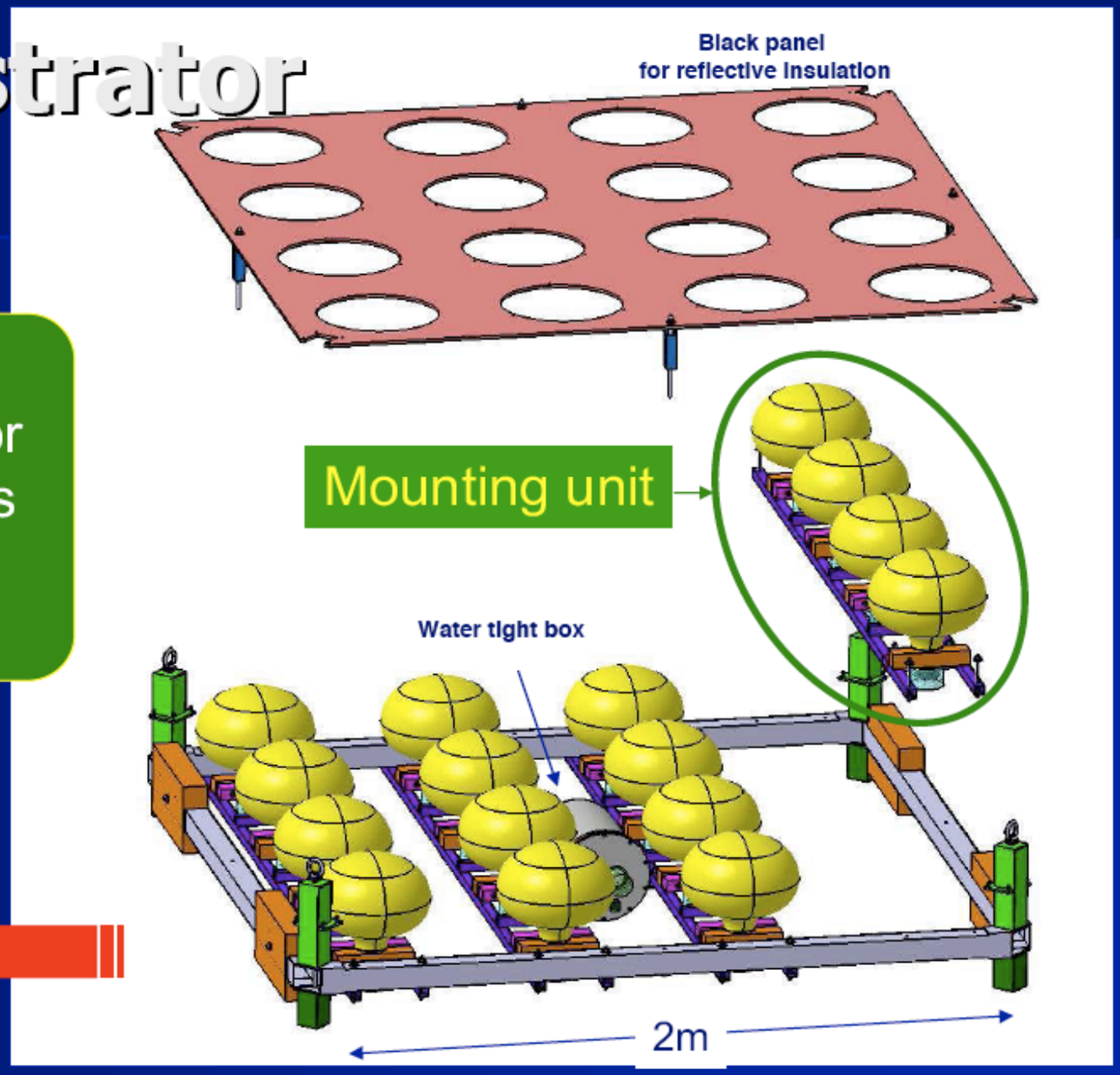
# Demonstrator Module

## Demonstrator

Design Ok
Construction Q4 2009

16 1” PM demonstrator in the 10bars BNL-IPNO vessel

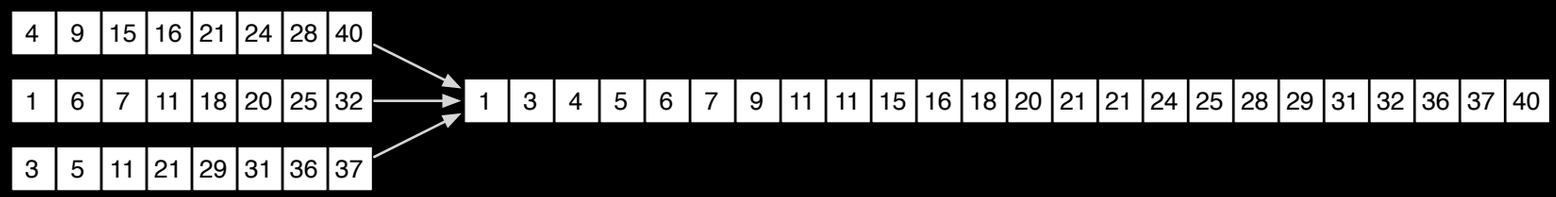
Compatible with MEMPHYNO water vessel (join LAL-IPNO-APC and ULB)




J.E Campagne Omega Users 2/07/2009

# DAQ Considerations

- Triggerless design → all data sent downstream and concentrated in single point. For MEMPHYS detector ~ 10 p.e. per MeV: some 50 p.e. spread over large area of detector at threshold - local triggering not possible.
- Assume 5 kHz background PMT rate.
- 56 bits data packet per hit - require data transmission rate of 5 Mbps per PMm$^2$ "box" over 100 m cable to *surface*.
- For $10^5$ ch - DAQ trigger must process $5\times10^8$ hits per second (28 Gbps) - this will require fast electronics with high I/O bandwidth.
- While the B/W scale is 100× greater - conceptually the design of such a system that assembles time-stamped data packets is embodied by the IceCube DAQ.
- We have developed a fast O(N logN) cascaded binary tree online sort in software however speed is currently at about 1 million sorts per second on commodity hardware.
- The algorithm is portable to firmware (no complex data structures).
- ULB has embarked on R&D with ATCA (Advanced Telecommunications Computing Architecture) for future DAQ deployments in HEP (sLHC / ILC) and astroparticle physics experiments.

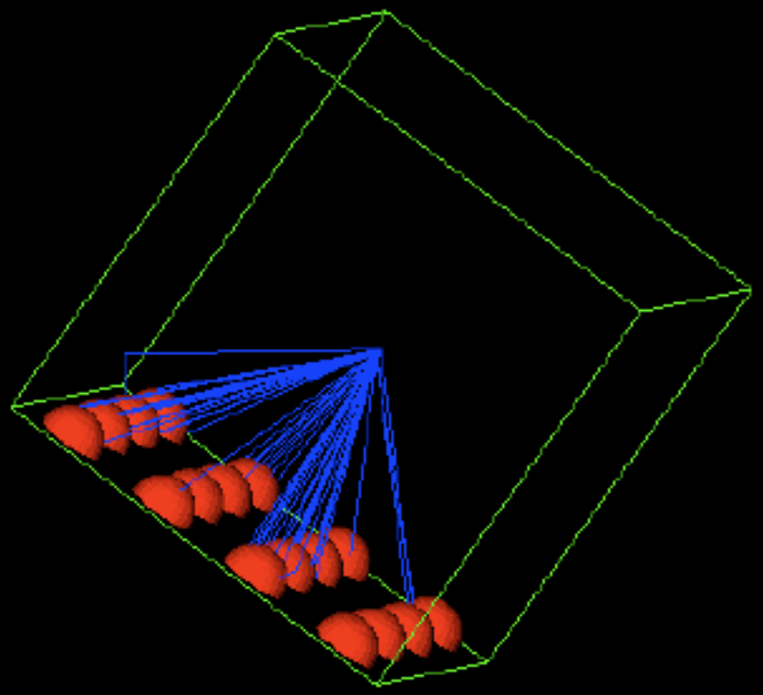


# Time Synchronization

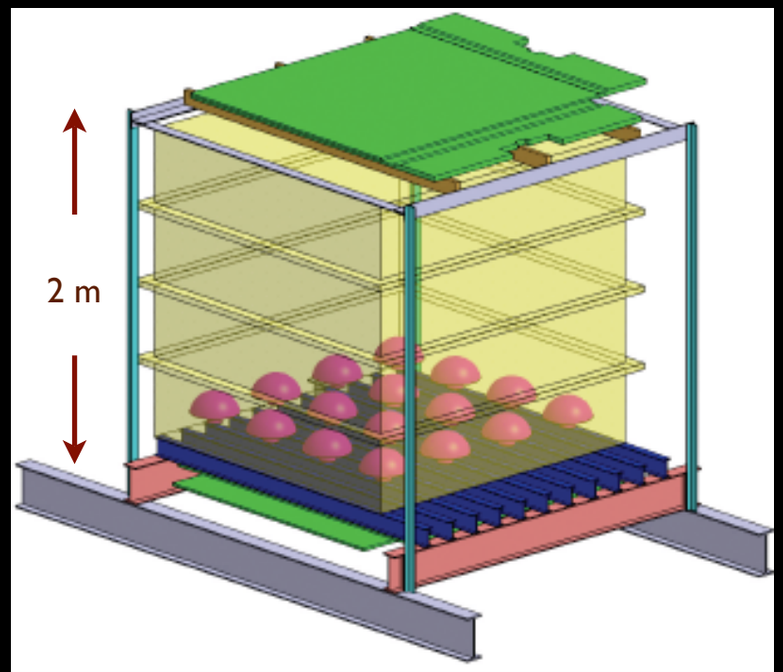
- Timing within group of 16 PMTs controlled by 10 MHz on-board oscillator + TDCs --> 1 ns resolution
- Between units need time synchronization system
  - In current hardware each PMm2 box accepts a 1 PPS signal which establishes a time frame reference for 24-bit time counter on PARISROC.
  - Must carefully set / measure pulse delays from master clock
  - Could add clock latch to remove any time frame ambiguity

# MEMPHYNO

Monte Carlo of 10 MeV $e^-$ in MEMPHYNO detector

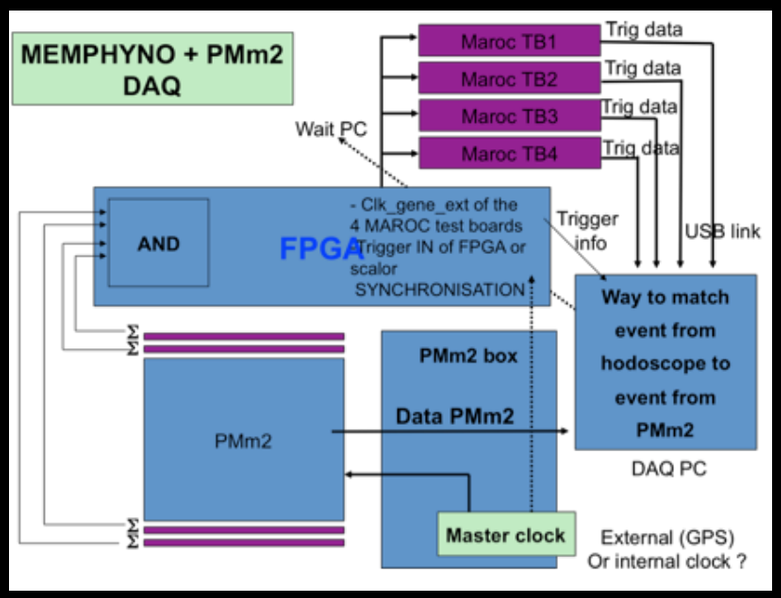


MEMPHYNO prototype tank under construction at APC (Paris 7)




MEMPHYNO goals - higher-level

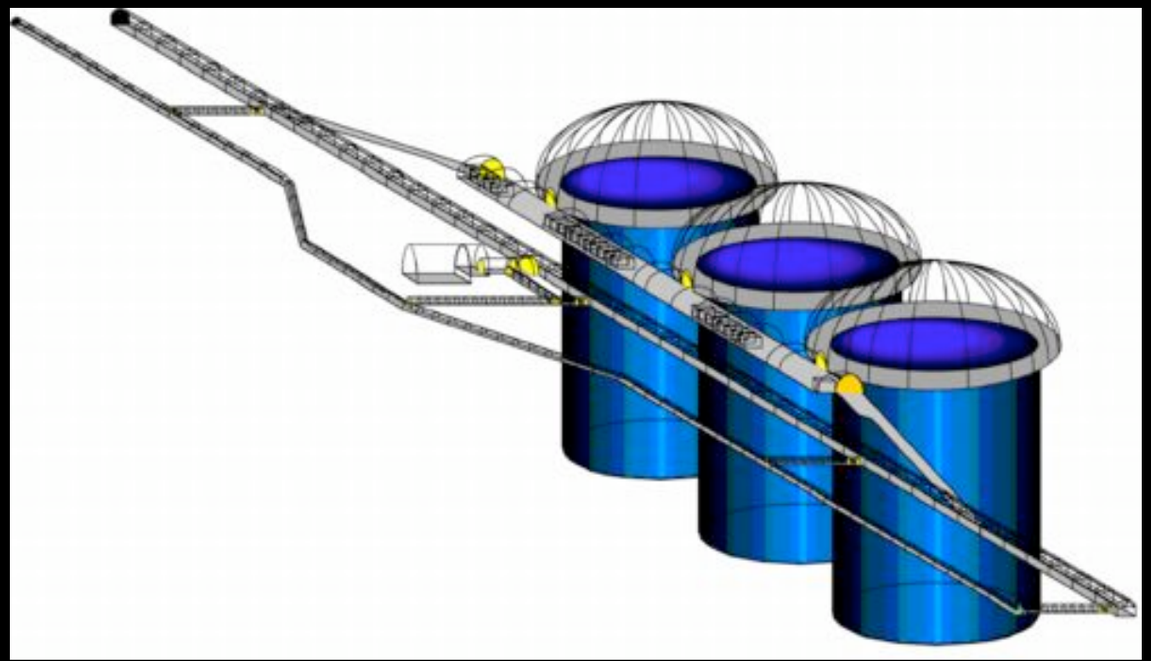
- Study PMT / $H_2O$ tank response to μ
- Evaluate ASIC performance / systematics under realistic signal conditions
- Reconstruct μ using PMT hits



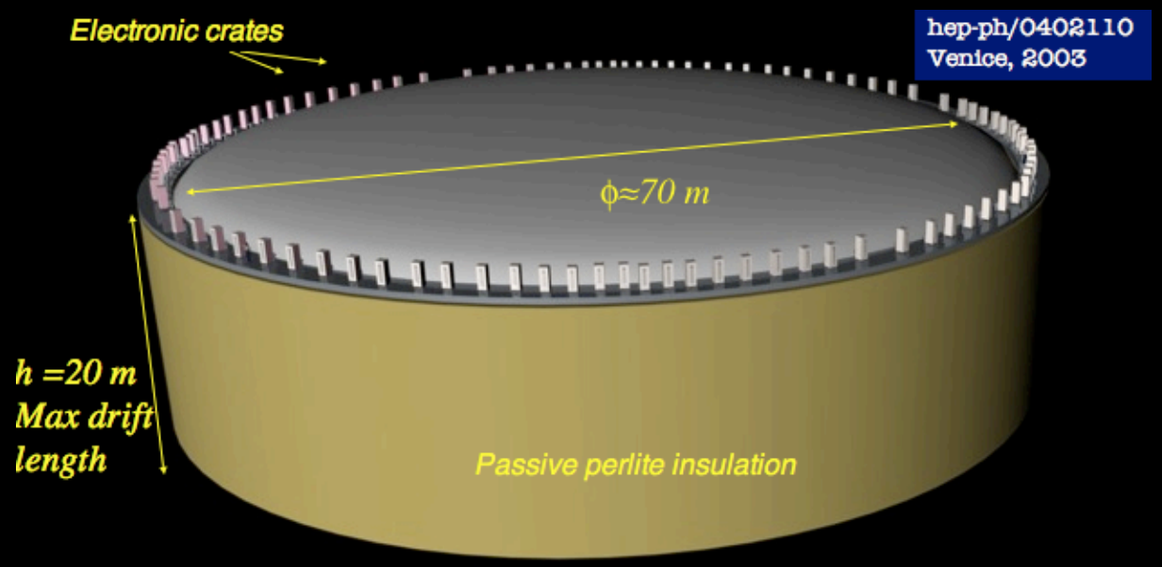



# Future

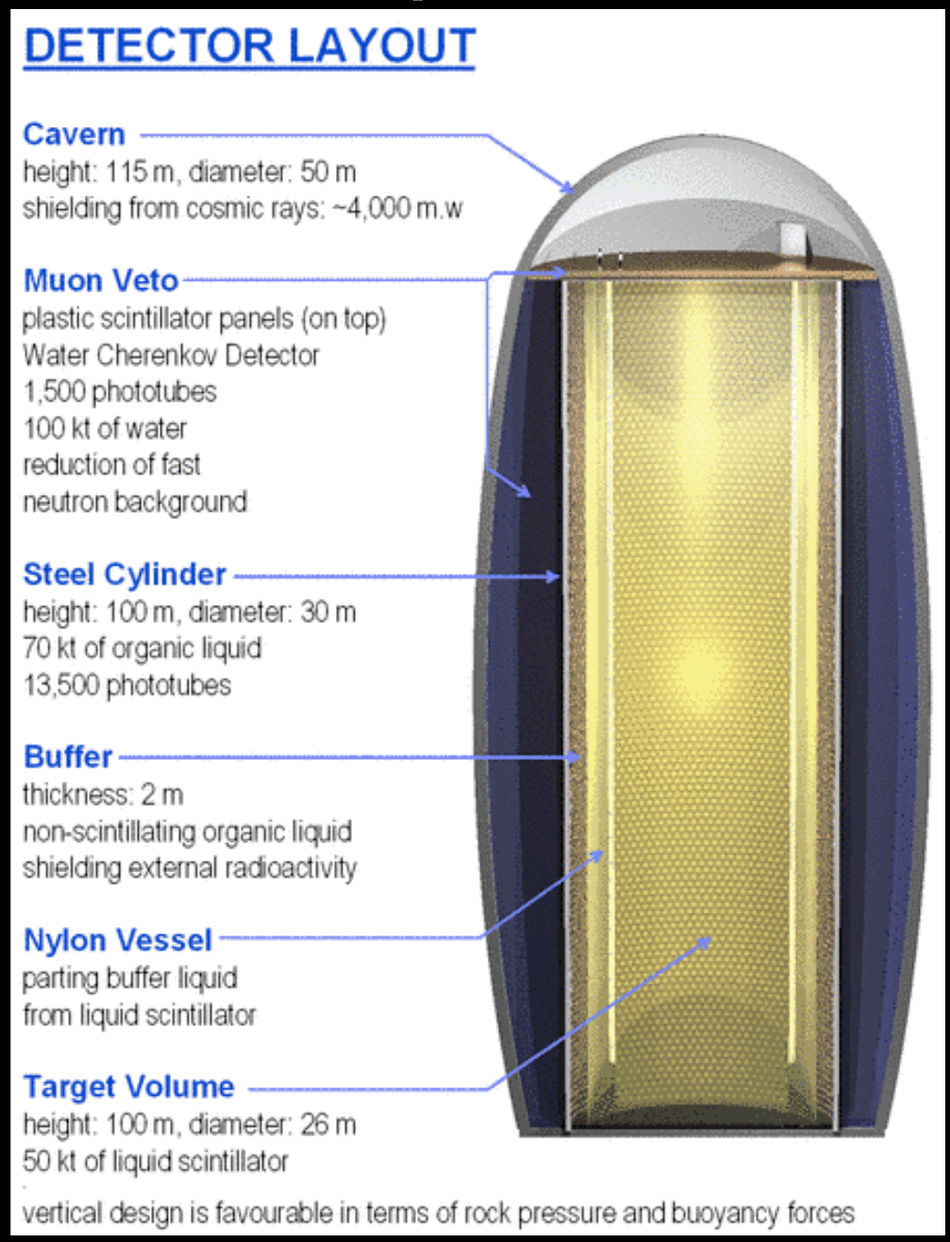
# LAGUNA



## MEMPHYS - $H_2O$




## LENA - Liquid Scintillator




## GLACIER - Liquid Argon

# LAGUNA - Site Selection

| | |
|---|---|
| LSM - Fréjus | France |
| SUNLAB | Poland |
| Pyhäsalmi | Finland |
| Slanic-Prahova Salt Mine | Romania |
| LSC - Canfrac | Spain |
| Boulby Mine | UK |
| CASO | Italy |

**Sept 2009**: LSM call for proposals J.E. Campagne LAL and T. Patzak APC will submit proposal to place MEMPHYNO prototype station in LSM tunnel.

# Wrap-up

- PMm$^2$ project will finish 25 July 2010 - 6 month extension granted by ANR due to Photonis departure
- Cessation of PMT activity by Photonis very sad news also for entire worldwide PMT 'community'
- Nevertheless, PMm$^2$ will complete build out of demonstration using 8″ Hamamatsu R5512 tubes.
- MEMPHYS : MEMPHYNO prototype under construction at APC.  Proposal to install in LSM test cavern underway.
- LAGUNA site selection due 2010