DOR <-> DOM Communication

A Short Overview & Test Results

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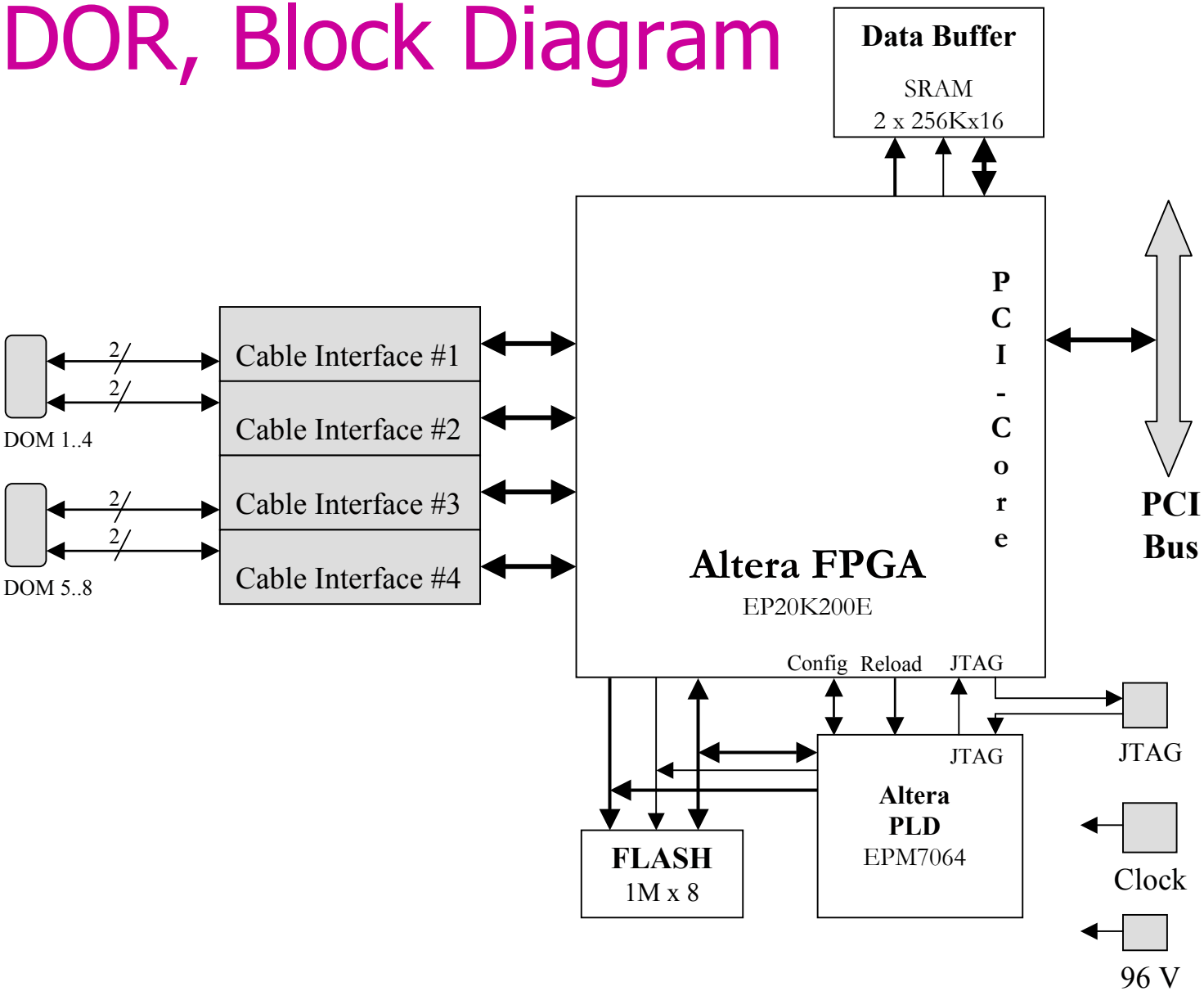
OSI (Open System Interconnect) 7-Layer Model

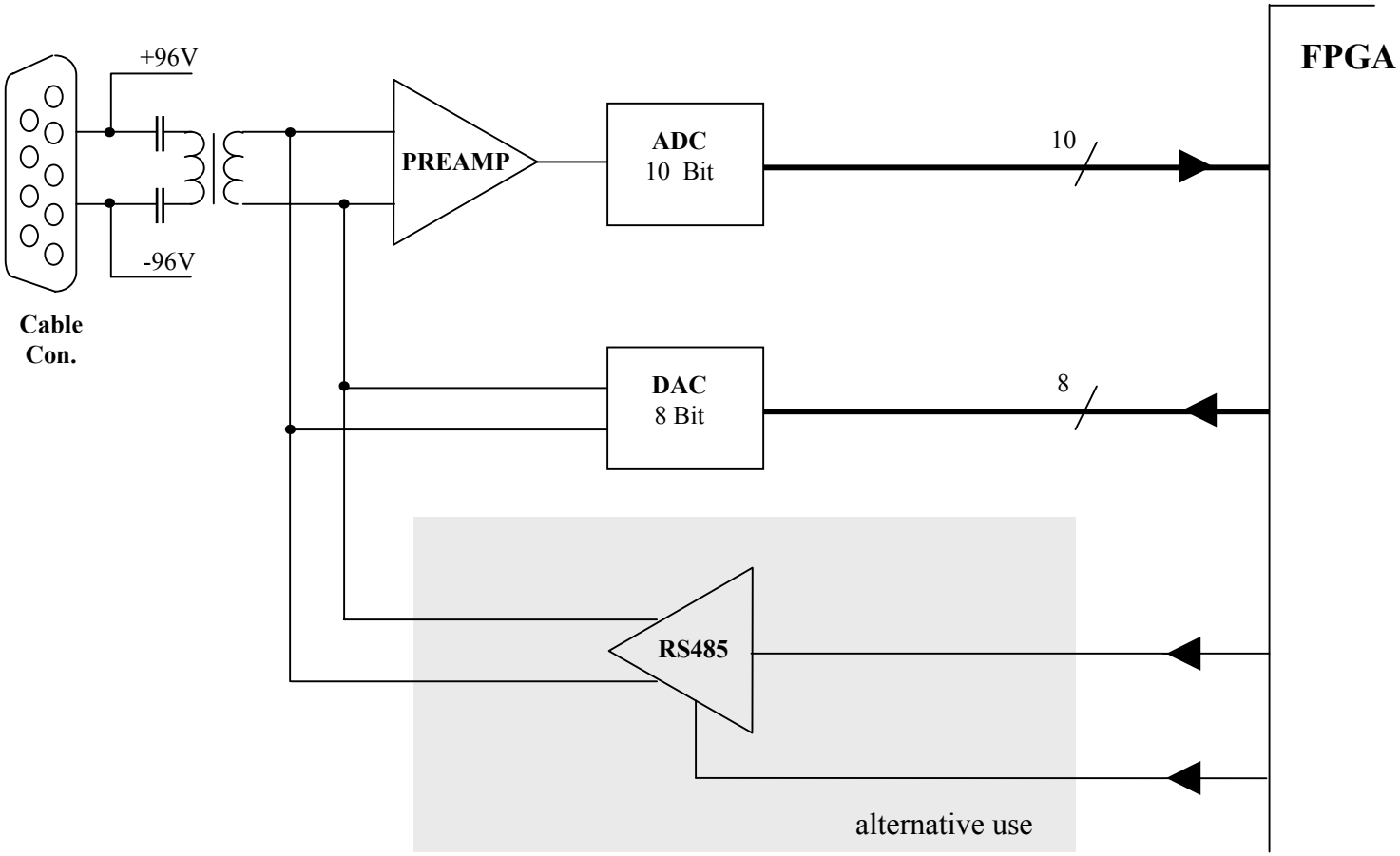
- Layer 2 by DOR firmware
- Physical Layer:
  - 140 Ω twisted pair cable
  - DSUB-9 connector
  - …
- Data Link:
  - UART like protocol
  - Half Duplex
  - Master / Slave
  - …

7	Application
6	Presentation
5	Session
4	Transport
3	Network
2	Data Link
1	Physical

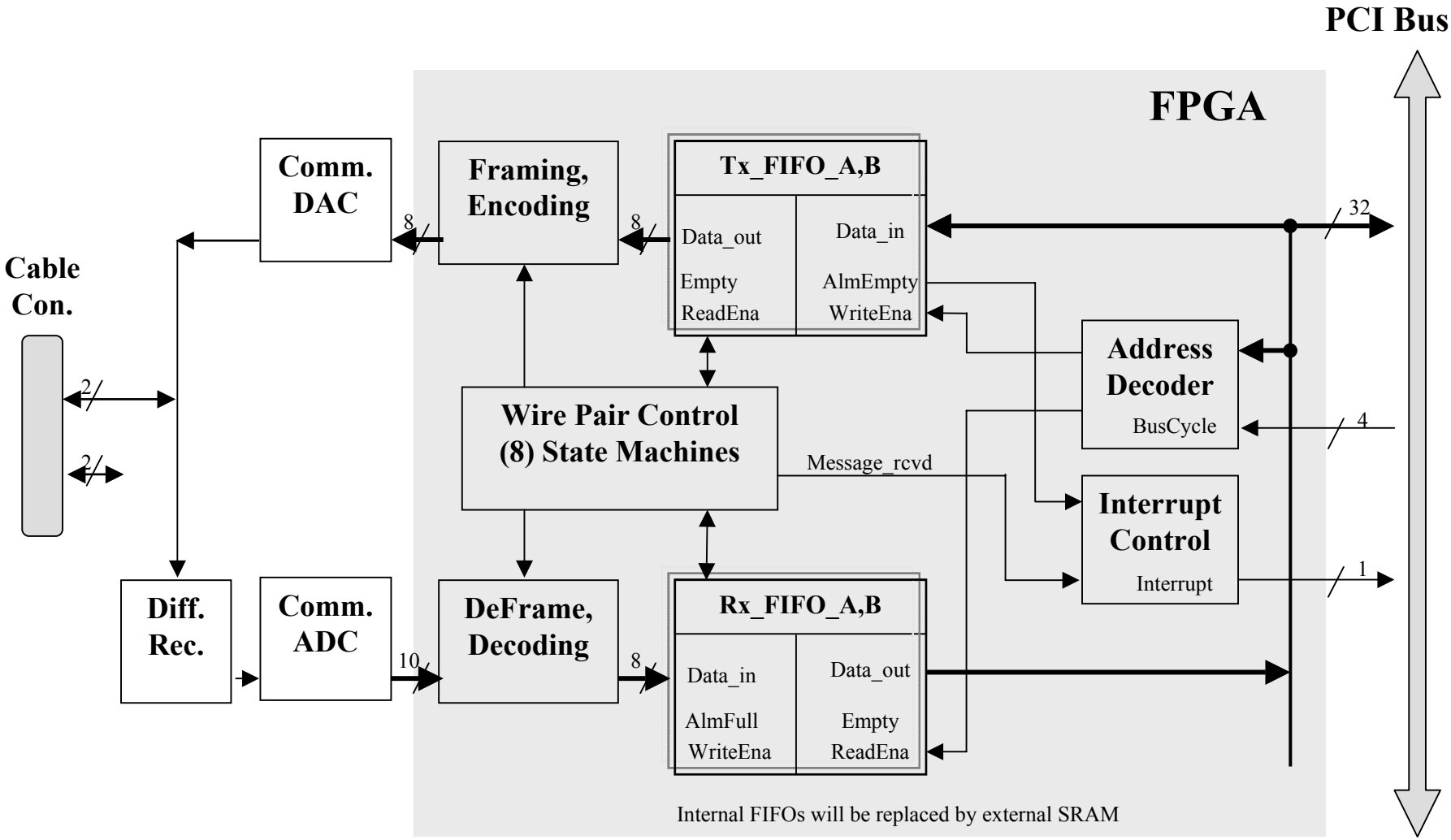
DOR, Block Diagram



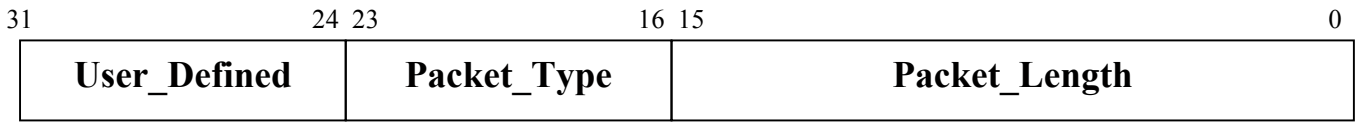
Cable Interface Scheme



Rx / Tx Data Path, one Wire Pair



Packet Header



Packet_Length: 0…65535, amount of bytes to be transferred

Packet_Type:

Encoding	Packet_Type
0x00	Data Packet (standard)
0x01	Time Calibration Data

User_Defined: not relevant for hardware

Packet Presentation

Example: Sending 7 bytes to DOM_B

32 bit Tx Buffer → Cable

Header	AB000007
1. Dataword	44332211
2. Dataword	00776655

85	*Start_Of_Frame*
AB 00 07 00	User_Defined Packet_Type Packet_Length_L Packet_Length_H
11 22 33 44	1. Dataword
55 66 77	2. Dataword
xx	*Packet_Number*
88	*End_Of_Frame*

incremental number
to detect lost packets

Green = Control bytes added by firmware

Byte Encoding

Data Byte

0	1	2	3	4	5	6	7	8	9
Start	**Data bits**								**Stop**
1	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7	**1**

Control Byte

0	1	2	3	4	5	6	7	8	9
Start	**Address**		**Command**				**Odd Par.**	**Tag**	**Stop**
1	Adr0	Adr1	Cmd0	Cmd1	Cmd2	Cmd3	**x**	**1**	**0**

Odd Parity of Adr0..1, Cmd0..3

Commands

Command	Encoding CMD3..0	Used by DOR	Used by DOM	Description
Not used	0000			
STF	0001	X	X	Start Of Frame
EOF	0010	X	X	End Of Frame
IDREQ	0011	X		DOM ID Request, needed ?
Not used	0100			
DRREQ	0101	X		Data Read Request (data polling)
DRAND	0110		X	Data Read Acknowledge, No Data aval.
DRBT	0111		X	DOM Rebooting
MRWB	1000		X	Message Received With (more) Buffer
MRNB	1001		X	Message Received No (more) Buffer
MRWE	1010		X	Message Received With Error
COMRES	1011	X		(DOM~) Communication Reset
BFSTAT	1100	X		(DOM~) Buffer Status request
SYSRES	1101	X		(DOM~) System Reset (Soft Boot)
TCAL	1110	X		Time Calibration cycle follows
IDLE	1111	X	X	IDLE, DOM answer on COMRES or IDLE

Command Sequence

DOR	**DOM**	**Description** (only one DOM is connected)
COMRES .. COMRES	 IDLE	After power on the DOR sends every 2 ms a COMRES until DOM sends an IDLE back.
DRREQ	DRAND	Data Read Request. The DOM has no data.
STF ... EOF	 MRNB	Start Of Frame, Data, End OF Frame. The DOR was sending a packet The DOM received error free, but has no more buffer
BFSTAT	MRNB	Buffer Status Request. The DOM still has no buffer.
DRREQ	STF EOF	Data Read Request. The DOM is responding with a packet.
BFSTAT	MRWB	Buffer Status Request. DOM buffer is available now
DRREQ	DRBT	Data Read Request. The DOM is rebooting now.
COMRES ... COMRES	 IDLE	DOM is rebooting. The DOR sends every 2 ms a COMRES . DOM is ready now (typical after 160ms).

DOM Reboot Problem

- After DOM power on the DOM is rebooting two times
- Every reboot means a FPGA-reload as well
- Problem: asynchronous loss of communication
- Solution: synchronization with the data polling, DOM may only reboot after answering on DRREQ with DRBT
- DOR stops **all** data transfer and sends COMRES until it gets an IDLE back

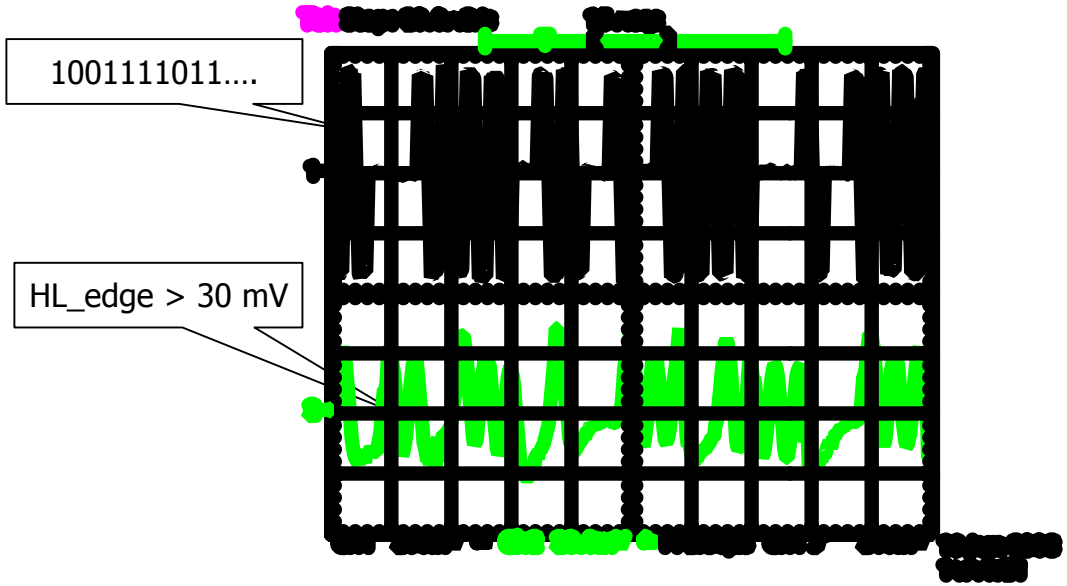
Tested Functionality

- Power On synchronization (COMRES command)
- DOM A/B data polling (DRREQ, DRAND)
- Framing and Deframing (STF, EOF)
- Prevention of DOM buffer overrun (BFSTAT, MRNB, MRWB)
- DOM Reboot handling (DRBT command)
- Automatically detection of a missing DOM -> full bandwidth dedicated to the other one
- SYSRES and TCAL not yet tested

Data Encoding

- DC-free bit encoding, 1MBit/s
- "0" = quiet line, "1" = bipolar rectangular pulse, T=1µs

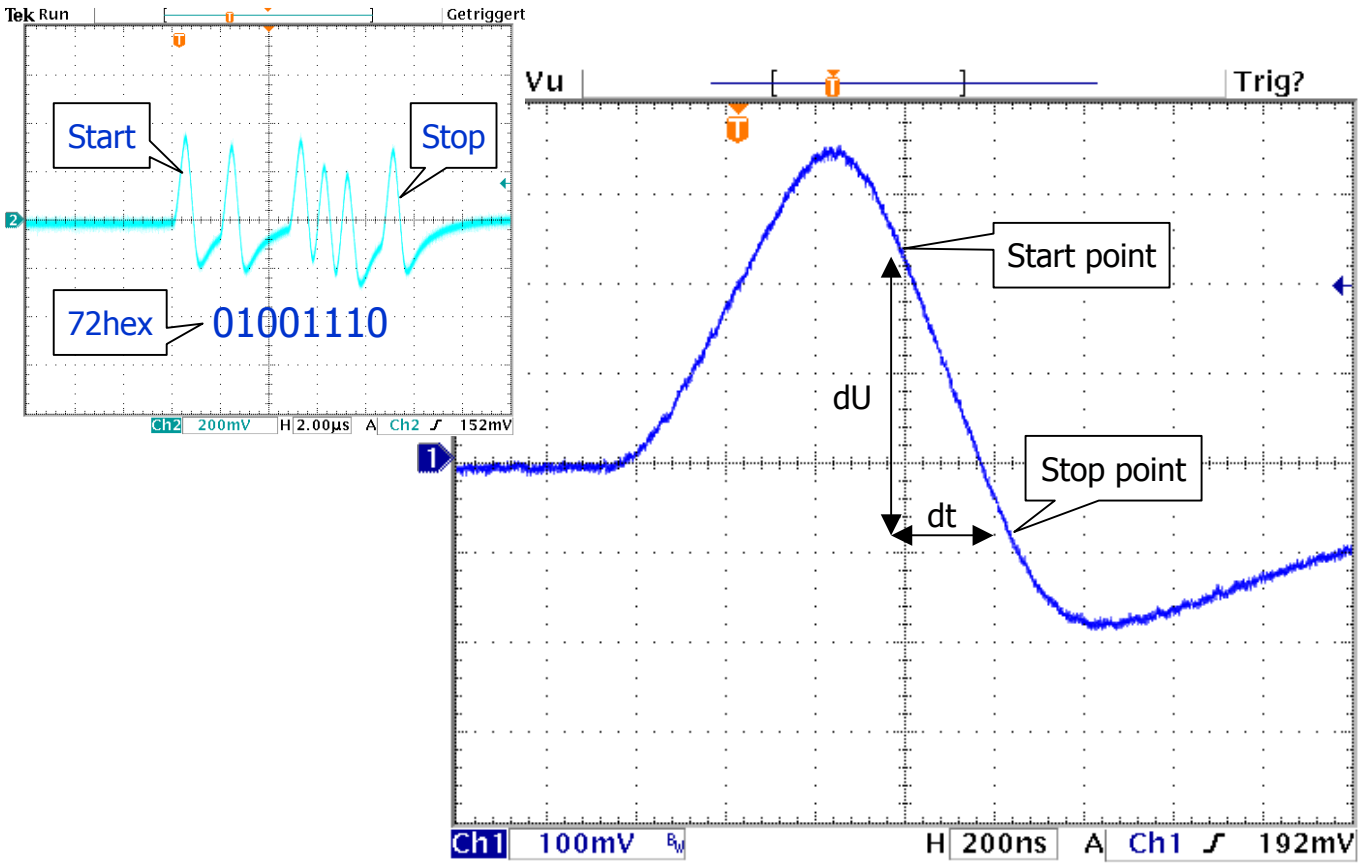
Tx (DAC) and Rx Signal using the new Ericsson Cable (3.4 km)



Measured between GND and one transformer tap using a Tektronix standard probe

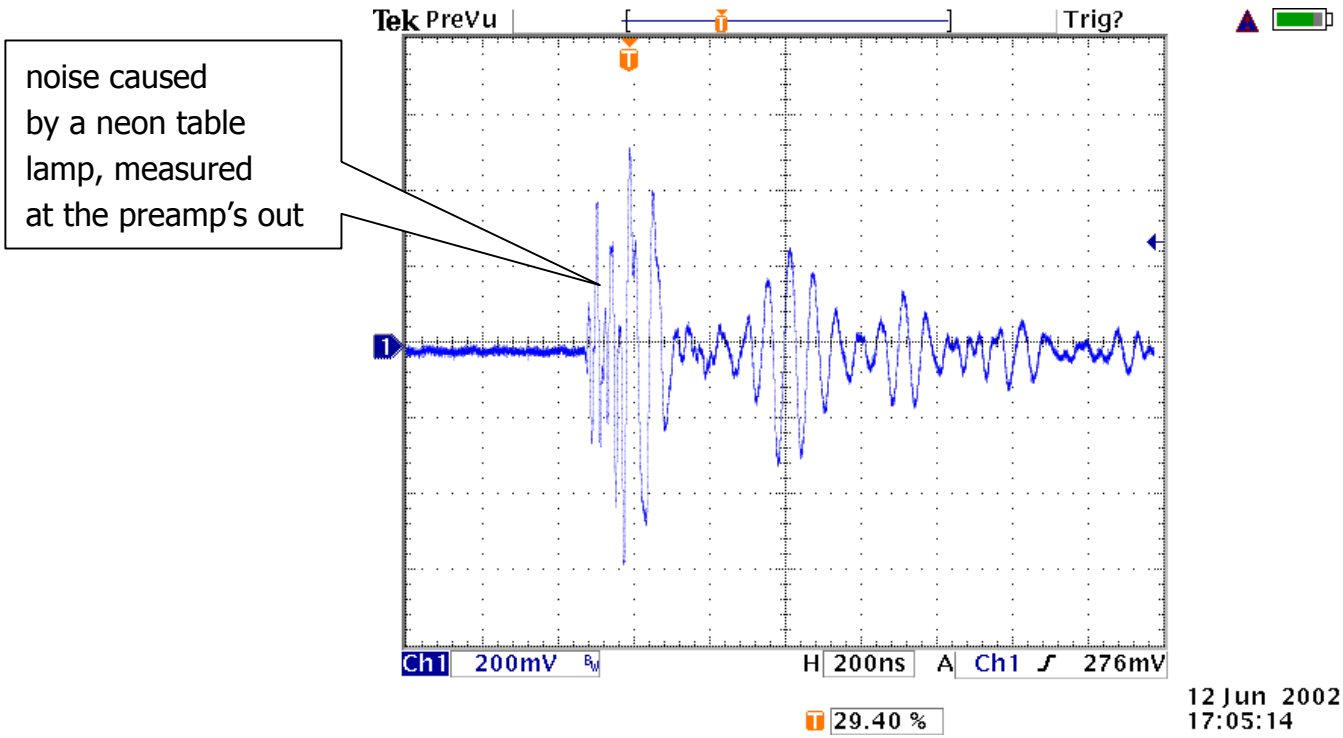
Digital Decoding

- evaluating the HL-edge in a time window to detect a "1"
- baseline correction not necessary



Noise

- problem: missing of a "standard" noise source
- noise by neon lamp starters and electrical engines used to evaluate the design progress



Digital Filtering

- simple digital mean value calculation over 4 ADC samples (bit time is 20 samples)

  $\text{mean}(adc[9..0])_i = (adc[9..2]_{i-1} + adc[9..2]_{i-2} + adc[9..2]_{i-3} + adc[9..2]_{i-4})$

  lower two bits not used, 0..3 -> 0..3mV
- goal is to eliminate high frequency noise spikes
- the filter algorithm is limited by the available FPGA resources
- Test using "natural" noise sources have shown a significant improvement
- more data security by decoding the stop bit
  - only if the stop bit has arrived the byte is written to the Rx FIFO
  - prevents zero bytes, caused by single noise spike-"start bits"

Status

- long term DOS-test with 4 DOMs (2 days, 3.4km new Ericsson cable, 48KB/s/DOM) error free under lab conditions
- DOM-Reboot needs still some debugging
- DOM Soft Boot (command SYSRES) still has to be tested
- Time calibration (command TCAL) not yet implemented

Next Steps

- DOM Soft Boot (command SYSRES) and TCAL test
- Debug FIFO to record the last 256 control bytes
- Possible improvements:
  - Adaptive edge decoder, especially for the DOM side (pk-pk value changes from 60mV to 1.2V, when a DOM is responding, but the other one is receiving)
  - Automatic adaption of the communication threshold after DOM power on
  - 8b/10b encoding scheme for better signal/noise ratio and/or higher data rates
  - 32 bit checksum implementation
  - Hardware initiated retransmit in case of an error