

DOR

DO_M Readout card

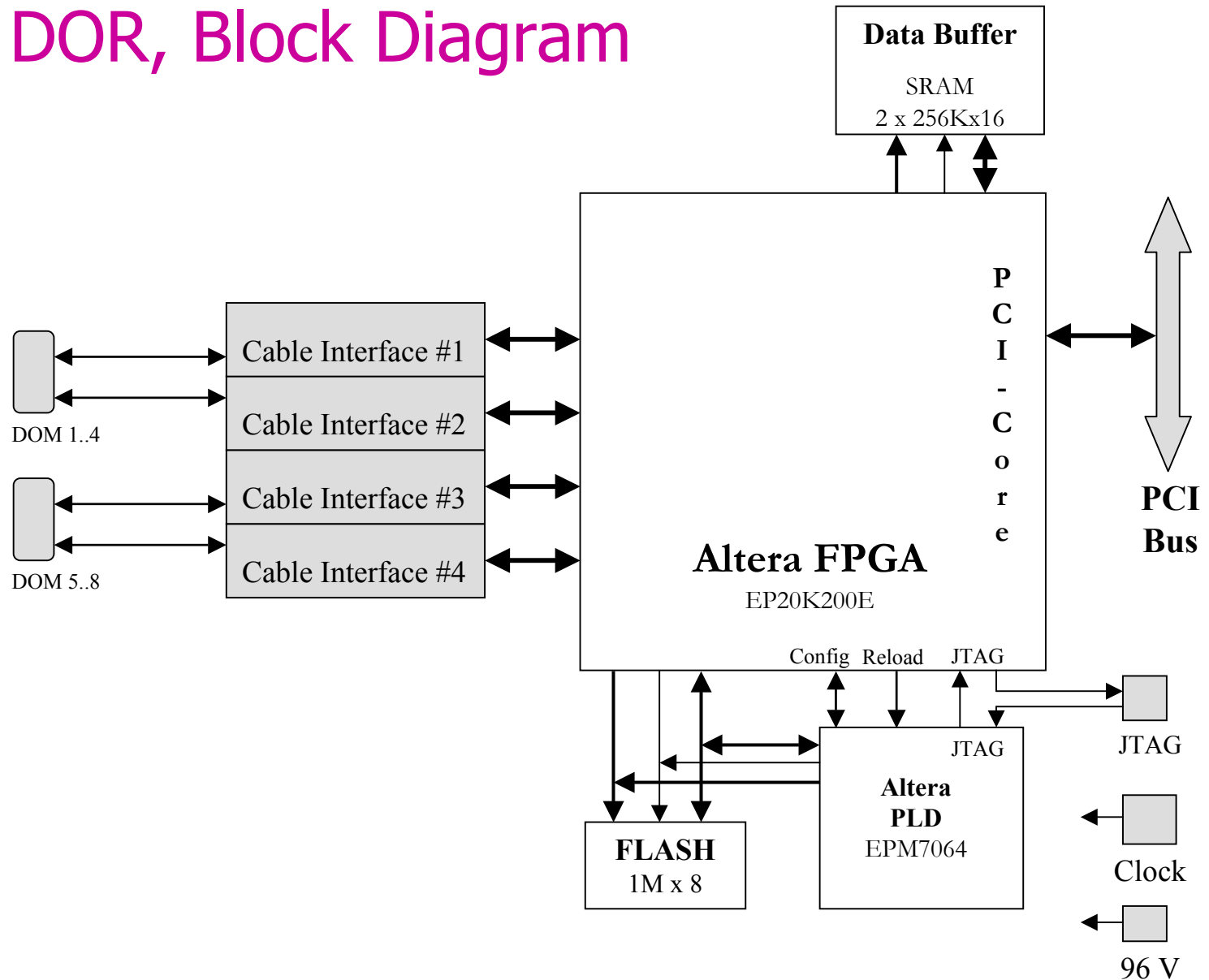
Status Report, November 2003

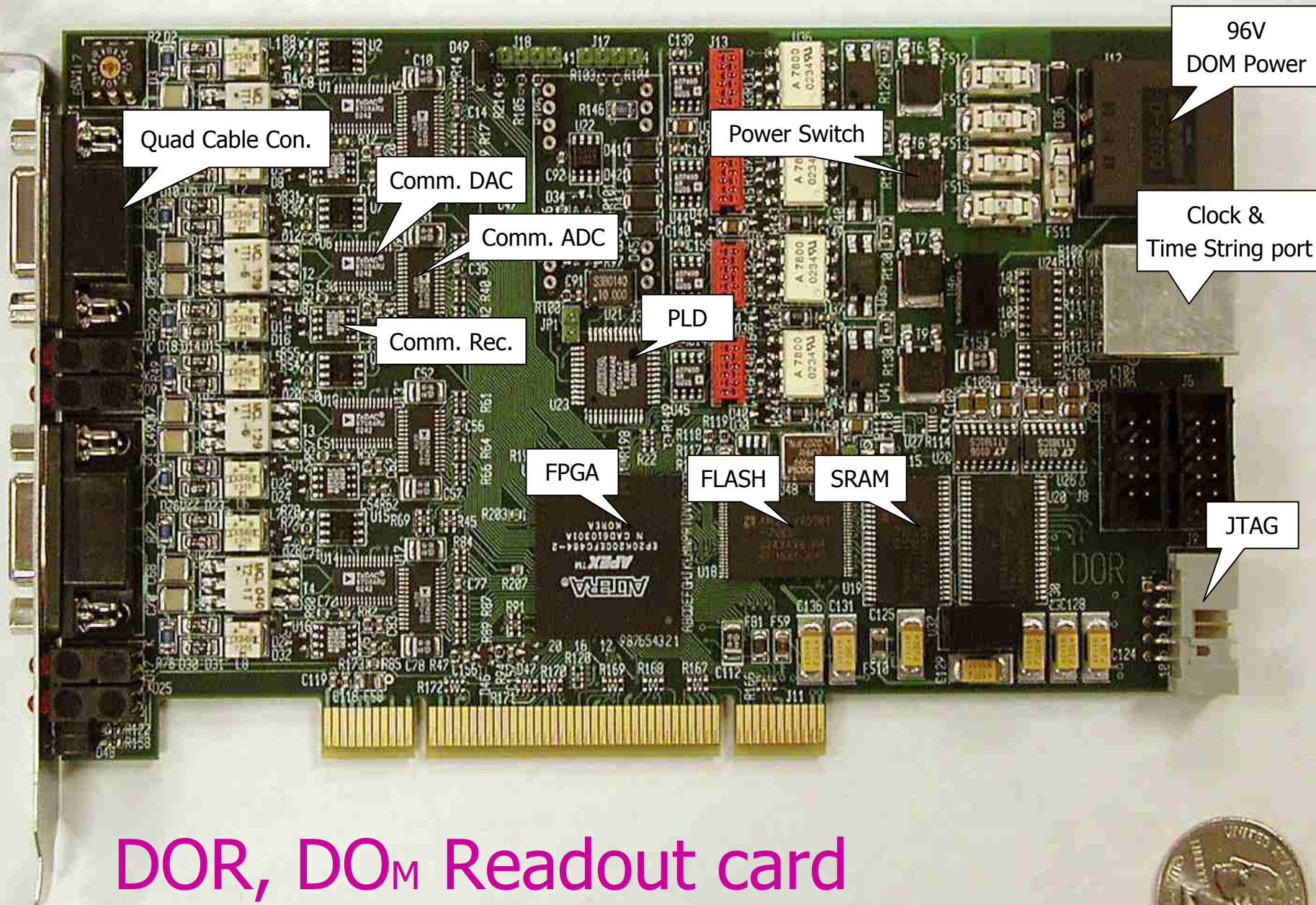
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DOR, Block Diagram





DOR, DO_M Readout card

DOM Hub

DOR card



Firmware Versions

- DOR_TEST
 - after production test
 - direct access to all HW components
- vDOM
 - Control of one wire pair + two virtual DOMs
 - Initial communication test
 - TCAL with same clock @ DOR and vDOM
 - for Linux driver test
- DOR
 - working version, under development

DOR Firmware Features

- PCI Bus control including DMA (..120 MB/s) & Interrupts
- In system firmware update w/o DOM hub reboot
- Parallel control of 2 wire pairs / 4 DOMs
- 1MBit/s serial data rate, (50KB per DOM)
- DOM_a/b polling
- DOM / DOR buffer synchronization
- Time calibration (TCAL data packet generation)
- Automatic cable length adaption (0.1m ... 3500m)

DOR Performance Test (DOS)

```
...Tx almost full flag detected, ttsizc = 00010000
...RESTORING (!!!) base_address_0 = D000

...DOR -firmware revision: 000.000.005.e
...DCOM -firmware revision: 017
...cable with wire pairs #0,1 detected, powering on now
...looking for DOMs, please be patient !!! It could take up to 4 sec

...DOM_A at LONG wire_0, ID=0013C629259, Iceboot (devel) build 293.....
...DOM_B at LONG wire_0, ID=0013C62A737, Iceboot (devel) build 293.....
...DOM_A at LONG wire_1, ID=0073C71D2EF, Iceboot (devel) build 293.....
...DOM_B at LONG wire_1, ID=0013C63B045, Iceboot (devel) build 293.....

...transfer & RAPCAL-test, TCAL-Period = 1000 ms, TCAL-cycles= 244845
...4 Bytes..504 Bytes (random P.length) of random numbers
...using Software-Datacheck, dom_7_0=0F
...Tx / Rx-Fifo access via DMA !!!
...ESC to break, CR for continuous run or any key for single step mode

...DOM_0, Kbyte transfered: 10095998 ,packets: 49998708 ,pending: 18
...DOM_1, Kbyte transfered: 10096688 ,packets: 49998798 ,pending: 18
...DOM_2, Kbyte transfered: 10096898 ,packets: 50003818 ,pending: 18
...DOM_3, Kbyte transfered: 10095238 ,packets: 50003818 ,pending: 18
```

DOR Firmware revision

DOM Comm.- Firmware revision

Cable detection

Cable length adaption

48 bit DOM-ID

Iceboot string

Time calibration

KB transferred, after 244845 sec,
244845 sec = 68 hours,

DOR Rev. 0, Performance

- PCI Bus , DMA with up to 120 MB/s
- 1MBit/s serial data rate, (50KB per DOM)
- Bit error rate $< 1 \cdot 10^{-10}$ (no error @ 100KB / 24h) @
 - 3400m new Ericsson cable, 35m off spool
 - 1 quad with 4 DOMs, random data / random packet length
 - Mix of comm. (echo-) test and TCAL (every sec)
 - Low noise office environment

Firmware Design, Next Steps

- DOM communication module
 - Data buffer, 2x1KB FIFO -> 2x16KB Dual Port RAM
 - CRC + packet retransmit
 - 8b/10b encoding
- DOR (additional)
 - Data buffer, FIFO -> External SRAM
 - DOM current measurement
 - HW based TCAL timer load
 - TCAL sequence with whole string comm. shut down

DOR Rev.1, Design Changes

- Bigger FPGA -> 2.5 x more logic cells and internal memory
- Symmetric DOM twofold power switch (+48V, -48V)
- New comm. transformer (same like DOM Rev.4)

Production Status, Rev. 0

- 10 DORs running at : UW 2x, Bartol 3x, LBNL 5x
- 20 more in production now, ready end of Dec. 2003
- Planned DOR-Rev.0 distribution (overall), Jan. 2004

UW	LBNL	Bartol	UP	DESY
8+3	8+3	2+2	2	2

Planned Production, Rev. 1

- PCB Rev. 1 ready in January
- first test in Feb., production of 60 if o.k.
- 60 DORs ready in April 2004
- 60 DORs -> sufficient to control 480 DOMs

Quality Assurance

- Robust PCB Technology chosen
 - 8 layer board
 - All contact areas gold plated
 - Traces, vias, distances “maximized”
 - Carefully chosen FPGA pinout (busses)
 - 100% hand routed to minimize via count
- ICs by “big” vendors only (if possible)
 - TI, AD, LT, AMD, National, Altera, ...
- Production quality check at the manufacturer

Documentation

<http://www-zeuthen.desy.de/~sulanke/Projects/>