DOR

DOM Readout card

Status Report, November 2003

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DOR, Block Diagram

Data Buffer
SRAM
2 x 256Kx16

DOM 1..4
Cable Interface #1
Cable Interface #2
Cable Interface #3
Cable Interface #4

DOM 5..8

Altera FPGA
EP20K200E

PCI Core

Cable Interface #1
Cable Interface #2
Cable Interface #3
Cable Interface #4

Config
Reload
JTAG

FLASH
1M x 8

Altera PLD
EPM7064

JTAG

PCI Bus

JTAG

Clock

96 V
Firmware Versions

- **DOR_TEST**
  - after production test
  - direct access to all HW components

- **vDOM**
  - Control of one wire pair + two virtual DOMs
  - Initial communication test
  - TCAL with same clock @ DOR and vDOM
  - for Linux driver test

- **DOR**
  - working version, under development
DOR Firmware Features

- PCI Bus control including DMA (..120 MB/s) & Interrupts
- In system firmware update w/o DOM hub reboot
- Parallel control of 2 wire pairs / 4 DOMs
- 1MBit/s serial data rate, (50KB per DOM)
- DOM_a/b polling
- DOM / DOR buffer synchronization
- Time calibration (TCAL data packet generation)
- Automatic cable length adaption (0.1m ... 3500m)
DOR Performance Test (DOS)

- DOR Firmware revision
- DOM Comm.- Firmware revision
- Cable detection
- Cable length adaption
- 48 bit DOM-ID
- Iceboot string
- Time calibration
- KB transferred, after 244845 sec, 244845 sec = 68 hours,
DOR Rev. 0, Performance

- PCI Bus, DMA with up to 120 MB/s
- 1MBit/s serial data rate, (50KB per DOM)
- Bit error rate < 1*10^{-10} (no error @ 100KB / 24h) @
  - 3400m new Ericsson cable, 35m off spool
  - 1 quad with 4 DOMs, random data / random packet length
  - Mix of comm. (echo-) test and TCAL (every sec)
  - Low noise office environment
Firmware Design, Next Steps

- **DOM communication module**
  - Data buffer, 2x1KB FIFO -> 2x16KB Dual Port RAM
  - CRC + packet retransmit
  - 8b/10b encoding

- **DOR (additional)**
  - Data buffer, FIFO -> External SRAM
  - DOM current measurement
  - HW based TCAL timer load
  - TCAL sequence with whole string comm. shut down
DOR Rev.1, Design Changes

- Bigger FPGA -> 2.5 x more logic cells and internal memory
- Symmetric DOM twofold power switch (+48V, -48V)
- New comm. transformer (same like DOM Rev.4)
Production Status, Rev. 0

- 10 DORs running at: UW 2x, Bartol 3x, LBNL 5x
- 20 more in production now, ready end of Dec. 2003
- Planned DOR-Rev.0 distribution (overall), Jan. 2004

<table>
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<th>UW</th>
<th>LBNL</th>
<th>Bartol</th>
<th>UP</th>
<th>DESY</th>
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Planned Production, Rev. 1

- PCB Rev. 1 ready in January
- first test in Feb., production of 60 if o.k.
- 60 DORs ready in April 2004
- 60 DORs -> sufficient to control 480 DOMs
Quality Assurance

• Robust PCB Technology chosen
  – 8 layer board
  – All contact areas gold plated
  – Traces, vias, distances “maximized”
  – Carefully chosen FPGA pinout (busses)
  – 100% hand routed to minimize via count

• ICs by “big” vendors only (if possible)
  – TI, AD, LT, AMD, National, Altera, ...

• Production quality check at the manufacturer
Documentation

http://www-zeuthen.desy.de/~sulanke/Projects/