Design Requirements for the

IceCube Master Clock System

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November 14, 2003

1. Introduction

This document attempts to capture both the system and subsystem requirements for the IceCube Master Clock Unit (**MCU**) subsystem. In addition, certain implementation issues need to be addressed now, because both IceCube DAQ architecture and design are relatively well-advanced.

The **MCU** subsystem of the IceCube DAQ is the source that provides the capability to ascribe to each "hit" detected by any of the ~5120 Digital Optical Modules (DOM a time-stamp common to the entire IceCube = InIce + IceTop array. This common time-stamp shall be referred to as **IceCube Time Calibration (ITC)**. The creation of the **ITC** requires a complex sequence of information capture at both DOM and DOM Hub. Ultimately, a transformation of local DOM clock data to **ITC,** using **MCU**-generated data, is made in the string processor. This process will not be described further in this note, except as needed for the requirements and justifications.

The **MCU** shall provide three information streams:
1. A high-stability **20 MHz clock signal**;
2. A **1 Hz pulse signal**, phase -synchronized tothe 20 MHz clock;
3. A **time value string (TVS),** updated at the1 Hz pulse.

The time value string **TVS** is naturally provided by a GPS source. A goal for the **MCU** is to exploit the information streams provided by GPS functionality while maintaining flexibility. The **MCU** frequency stability requirement introduces some complexity, as the **MCU** must also avoid an inherent limitation in the short-term GPS stability. The frequency stability issue prevents an exact equivalence of **ITC** and **GPS** time

For many test purposes it is also desirable to have the capability to operate a DOM Hub without the **MCU** subsystem, *i.e.,* to use a GPS source instead, or even in stand-alone mode, *i.e.,* to run with no GPS source. At the same time, there is motivation to keep the design of the **MCU** subsystem as simple as possible.

In the IceCube DAQ architecture, the DOM Hub is the subsystem that controls and maintains the essential **ITC** functionality for all DOMs in the array. To perform this function, each DOM Hub receives the three information streams from the **MCU** subsystem. The interaction between the **MCU** and the DOM Hub is referred to in this

note as the ***ITC** process*, whereas the *time calibration process* for the DOM local clocks is a different and distinct process. The term *synchronization* will be used to define sequencing of activity within the DOM Hub, as a means to mitigate cross-talk effects. There may be a need to refine nomenclature in this area.

Within the DOM Hub, there are two custom design elements integral to this function, the **DOR** card and the DOM Hub Service Board (**DSB**). The **DOR** card has already been designed by K-H Sulanke of DESY, and performance meets expectations. The **DSB** is at an early stage of design. It will provide a fan-out for the **MCU** signals to the **DOR** cards, as well as a local 20 MHz clock for autonomous testing purposes. The **DSB** also provides various DOM Hub monitor functions unrelated to the timing purpose, such as determining whether crate power is present, DC power levels OK, etc. The **MCU**, the **DOR** cards, and the DOM Hub Service Card (**DSB**) are the only active elements of surface DAQ which must control, distribute, and measure timing at the nanosecond level.

The DOM Hub implementation concept was developed by K-H Sulanke (DESY). It consists of an industrial PC enclosure, a standard backplane with PCI bus, a CPU for control and data flow , eight **DOR** cards, one **DSB**, + various power supplies, disk, fans, *etc.* The present working plan is that DESY will take responsibility for the design (fabrication) of both the **MCU** and the **DSB**, following the approved requirements document and implementation plan, and that K-H Sulanke (DESY) will undertake the design task.

2. System Requirements

- **Verification:** All DAQ subsystem elements involved in generating or capturing **ITC** shall be verified for correctness once each second, and the tests shall have redundancy sufficient to determine the source of error.

  Justification: The process of creating the **ITC** is a complex sequence of actions, and the corruption or absence of correct **ITC** results in immediate and fatal corruption of data. The need to establish correctness of operation is clear, and once each second seems natural, since the new GPS time is available at this rate.

  Discussion: Reasonable people may differ about the level of redundancy needed for verification. In the more conservative perspective, the value in every **DOR** timer is tested at 1 Hz, comparing the current value at the instant of the 1 Hz pulse arrival with the new representation of the time value string (**TVS)**. A further check is possible by testing that the difference between the old and new values corresponds to exactly to the clock frequency, 2×10^7 Hz. The MCU can verify that the three GPS clocks agree, providing a further check. The MCU can also count the output streams of the 10 MHz atomic clocks and compare these. The optimum verification algorithms will require further study.

- **Initialization:** The **MCU** and the DOM Hub shall be capable of establishing the **ITC** process and data stream without direct high level DAQ software intervention to establish this process throughout the DOM Hubs.

Justification: The initiation of counting, which must occur simultaneously - at the same 50 ns clock tick in all **DOR** cards within the system - is not gracefully done with software since latencies are not controllable or stable. Software can, however, be employed to send a permission grant command to the **MCU/ DOM Hub** to permit counting to start, but the **ITC** process shall not depend on the timing of these global DAQ commands.

Discussion: It is proposed by K-H Sulanke that the **DOR** card timer be set, at the 1 Hz pulse rate, to the latest **TVS.** The **TVS** is an ASCII string defining GPS to the second. No conversion of this string by the **MCU** or the DOM Hub is necessary, since this information is not exploited until the string processor performs the transformation to ITC. The fractions of each second are in units of 50 ns, corresponding to the clock frequency of 2×10^7 Hz. Thus the **DOR** timer need only count from zero to 2×10^7. To record this information, only 24 bits are necessary. The **DOR** card must associate the ASCII **TVS** data with the DOR timer data when performing the RAPCAL function.

- **Absolute accuracy of time distribution:** The propagation time of the timing signals from the active GPS source to the **DOR** card FPGA input pins shall be determined with an error not to exceed 5 ns.

Justification: To provide an ultimate, or universal time value for events in the ice, it is necessary to know the propagation times for signals through the **MCU**, the **DSB**, and the **DOR** card. The RAPCAL process will determine the propagation time through the cables. The total propagation time for GPS through the system to the DOM adds a delay, which is measurable and stable. The uncertainty in this propagation time is distinct from the intrinsic GPS errors. This absolute time uncertainty should not be confused with the DOM local clock calibration error, which has a similar numerical value.

- **Autonomous behavior:** The system will allow all **DOR** cards servicing a single string to perform synchronized time calibrations of all attached DOMs without real-time intervention by either the DOM Hub CPU **DOR** card driver or the DOM Hub application.

Justification: Cross-talk within the main cable may require synchronized time calibration operation of the DOM Hub. In order to minimize the communications deadtime required to perform synchronized time calibrations across an entire string, **DOR** card activities must, in this case, be carefully and efficiently sequenced. The efficiency required to keep the communications deadtime to approx. 50 msec. per calibration is difficult to obtain through any software mechanism executing on the DOM Hub Linux system. Therefore, it is preferable to have this mechanism completely contained within the **DOR** card hardware and firmware.

• **Independence:** The **ITC** process for each DOM Hub will be independent of the state of other DOM Hubs, if any, in the system.

> Justification: During some phases if DAQ operations (e.g. deployment), DOM Hubs will be added to the system and possibly be rebooted a number of times. It is essential that individual DOM Hubs can achieve **ITC** with out affecting, either directly or through the intervention of the DAQ control program, the existing **ITC** process or operational state of other DOM Hubs.

- **Standalone Modes:** The DOM Hub shall be capable of operating, for certain test purposes, with a standard GPS source as a substitute for the **MCU**. In addition, it shall be possible to operate with no GPS unit in operation, using the **DSB** local 20 MHz oscillator.

> Justification: Debugging and test activities through out the IceCube collaboration will involve the use of DOMs and DOM Hubs. Many of these activities will not require the precision of the **MCU** subsystem.

3. MCU Subsystem Requirements:

• **Frequency/Phase Stability:** The **MCU ITC** shall display a short-term frequency stability $\delta f/f$ not worse than 1×10^{-11} (maximum - not rms) in a ten-second interval.

> Justification: The DOM clocks are expected to display short-term frequency stability in the range of $\delta f/f \approx 1 \times 10^{-10}$ in a ten-second interval, perhaps even significantly better. It is reasonable to require that the contribution of the **MCU** frequency drift to the measured distribution of calibration errors for the ensemble of DOM clocks be less than 10% of the σ of this ensemble time calibration error distribution. This will ensure that the period between calibration procedures will be determined solely by the DOM clock ensemble. GPS sources, however, display short-term stability not better than $\sim 4 \times 10^{-8}$, significantly worse than the performance expected for DOM short-term stability.
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> **Discussion:** This stability requirement implies that the direct, unpolished, output of GPS sources is inadequate, even under ideal circumstances, and that a frequency source with superior short-term drift is required, *viz*, an atomic stabilized clock.

• **GPS source degradation:** To accommodate degradation of GPS time value quality, due to technical difficulties or for any other cause, a frequency source capable of providing continuous output of the high-stability 20 MHz and 1 Hz signals for indefinite periods is required as an integral part of the **MCU**. This frequency source shall also be capable of providing long-term concordance with a GPS time value source, while maintaining the short-term frequency stability defined in the first requirement.

Justification: GPS units provide information about the quality of the calculated time value. Nothing is known at the moment about the quality of GPS data observed at pole, although a query might produce such information. Very low drift atomic clocks with 10 MHz signals are a natural solution to this requirement, and are commercially available at reasonable cost in compact packages. The lifetime of such atomic clock units is also expected to be at least 10 years.

- **GPS source loss:** In the event of loss or absence of GPS information or signals, the system will maintain **ITC** operation, when properly configured. There shall be no interruption of **MCU** and DAQ service when switching into a non-GPS mode, with the exception that the accuracy of the **ITC** time value will be allowed to drift without requiring GPS concordance.

  Justification: There may be circumstances, *e.g.*, political crises, during which GPS time signals may become unavailable for an extended or arbitrarily long period of time. The **MCU**, and the IceCube array, must be able to continue operation during such intervals and produce data of the same quality as that produced when GPS signals are available. The quality of data will not suffer, except that the precision of the time relationship to data from other unrelated detector systems will be lost. The **MCU** may be programmed to create a dummy GPS **TVS** field in this case, accompanied by a quality character to denote this.

- **GPS Redundancy:** The **MCU** will provide for the simultaneous operation of three GPS units, of which at least two shall be compared continuously for exceptions, quality, and error conditions. At least one unit shall be available as cold standby. Any one of the hot GPS units may be selected to serve as the time value source for the **MCU**.

  Justification: The GPS units provide essential data through a hidden layer of substantial technical complexity. Comparison of **time value** data between units should indicate if a problem exists. The cost of providing for three,units, *a priori*, in the design is insignificant.

  Discussion: It is also possible to define logic within the **MCU** FPGA that can detect discrepancy among three hot GPS units, while monitoring the GPS quality character. It is conceivable that the MCU logic could switch automatically to a unit displaying the best quality character, but the prudence of this may be questionable.

- **Frequency source redundancy:** The **MCU** will employ three high-stability frequency sources. Two shall be in operation and which shall be compared continuously for differences. The remaining one shall be available as cold standby.

  Justification: High-stability frequency source units, such as atomic rubidium stabilized oscillators, provide essential signals through another hidden layer of substantial technical complexity. Comparison of signals between the two hot units should indicate the presence of a problem.

Discussion: How this comparison should be done most usefully needs further attention.

- **Relative phase accuracy at source:** The relative signal skew at the output ports of the **MCU** of the leading edge (50% level) of the 20 MHz signals will not exceed 0.4 ns min/max.

  Justification: The timing error budget allocates 1 ns min-max for the entire **MCU** error distribution. This is only one part of the distribution network. Modern device performance falls into this range, so this is not unreasonable.

- **Relative accuracy of time distribution:** The relative signal skew at the input ports of the DOM Hub of the leading edge (50% level) of the 20 MHz and 1 Hz signals will not exceed 0.7 ns min/max.

  Justification: The timing error budget allocates 1 ns min-max for the entire **MCU** distribution. This is only one part of the distribution network. Modern device performance falls into this range, so this is not unreasonable.

- **Relative accuracy of time capture:** The relative signal skew at the input pads of the **DOR** card FPGA of the leading edge (50% level) of the 20 MHz and 1 Hz signals will not exceed 1.0 ns min/max.

  Justification: The timing error budget allocates 1 ns min-max for the entire **MCU** error distribution.

- **Output redundancy:** In addition to the ports needed for both InIce and IceTop, the **MCU** distribution network shall be constructed with 8 additional output ports to provide redundancy in the event of single port output failure, and to provide other IceCube subsystems, AMANDA, and subsystems undefined at present, access to the master time data source.

  Justification: There will surely be a need for extra outputs, which cannot now be foreseen, and the cost of implementation is negligible. Extra outputs also provide useful redundancy in the event that circuitry in some channel(s) goes bad.

4. Discussion:

The following subsections elaborate further on various proposed requirements and issues.

GPS Source and Phase Stability:

A GPS source generates three distinct signals. From the current satellite mix a GPS source generates a 10 MHz clock output, a 1 Hz phase-synchronized pulse, and a GPS time string in ASCI characters (the value is one second later than actual true time). The

GPS short-term clock phase stability is dependent upon the available satellite mix, which is changing on the time scale of minutes. The GPS phase drift may be in the range of ± 20 ns on this time scale, perhaps even more. This is significantly poorer than that expected for the DOM local clocks, for which a typical stability may be $\delta f/f \sim 1 \times 10^{-11}$ per second.

High-Stability Frequency Source:

For this reason, it is necessary for the **MCU** to employ an atomic clock, which will provide excellent short term stability. A typical rubidium-stabilized clock, for example, will display a stability of at least one order of magnitude better than the DOM local clock in the span of a few seconds. In this latter case, measured drifts and calibration data for the DOM local clocks will be dominated by their own characteristics, rather than that of the source. Commercially available rubidium-stabilized clocks accept the 1 Hz GPS signal to guarantee long-term concordance through a slow thermal feedback mechanism. The outputs of the atomic clock are a 10 MHz clock signal and a phase-synchronized 1 Hz signal, mimicking two of the three GPS outputs. The ASCII time value string must be taken directly from the GPS unit for conversion and distribution. When slaved to a GPS unit, the atomic clock when first powered up will not be in concordance with the GPS unit, but, after a few minutes the 1 Hz signal will "jump" to the closest 10 MHz tick when nominal stability is reached.

Master Clock Subsystem Functionality:

From the atomic clock 10 MHz output, the **MCU** shall generate a phase-accurate 20 MHz reference frequency (frequency doubling to 20 MHz is needed for waveform sampling by the **DOR** card communications FADC). The 1 Hz phase-synchronized timing pulse from the atomic clock can be used directly. The **MCU** shall present these signals and the **TVS** time value string signals to a front- or rear-panel fanout. The allowable time skew for the 20 MHz and 1 Hz signals through the distribution network - from the **MCU** input clock port to the FPGA pins within the **DOR** card - is constrained to contribute less than 1 ns min-max to the timing error budget. The **MCU** - DOM HUB distribution network links may, however, be as simple as standard ethernet cables. A DOM Hub Service card within the DOM HUB distributes both the 1 Hz and 20 MHz signals to the **DOR** cards with tightly constrained edge time skew.

The TVS time string is also fanned out by the DOM Hub Service Board **DSB** to the **DOR** cards to facilitate the robust association to DOM local clock time. The distribution of TVS time value string, however, does not require ns time accuracy as the string value is serially received and simply stored in a register.

DOR Card Time-Base:

Each **DOR** card maintains an internal counter, called ***DOR** timer*, which increments at the 20 MHz frequency, *i.e.,* every 50 ns. The ***DOR** timer* counter is at least 24-bit binary. The ***DOR** timer* counter value, at the instant determined by the 1 Hz signal, must be compared each second for a match to the expected value, 2×10^7. At this same instant, the **DOR** timer register is reset to zero.

As discussed in the IceCube PDR, and elsewhere, the transformation to **ITC** time from DOM local clock time is made within the *string processor*. This transformation is performed on the coarse time-stamp for each "hit". The parameters for the transformation are dynamically derived using data obtained periodically by the **DOR** card and DOM (the **r**eciprocal **a**ctive **p**ulsing (**RAPCAL**) calibration methodology developed by Bob Stokstad *et al*). The **MCU** has no direct interaction with this process; it simply generates and distributes the (GPS+atomic clock)-derived timing signals and strings to the DOM HUBs.

Implementation:

The **MCU** distribution system is thus foreseen to consist of:

1. A box with 80 + 8 + m (m = number of ports needed for IceTop) output ports for the timing signals and GPS time value strings, with phase-synchronized inputs from three identical GPS units;
2. A set of three identical GPS units, which may or may not be housed within the box.
3. A set of three atomic-stabilized clocks, such as a commercial rubidium unit. Two of these shall be powered, to permit comparison of signals. A third redundant unit shall be made available in the same enclosure, and remain un-powered until needed.
4. A set of matched links from the **MCU** box to the DOM HUBs. These could be ethernet cables, or, conceivably but much less likely, optical fiber links, if noise is a problem.
5. A DOM Hub Service Board within the DOM HUB to ensure synchronous distribution to the **DOR** cards of the timing pulses and the time value strings.