Nanosecond-pulse generator for laser diodes

L. Howard and K. Daneshvar

Department of Electrical Engineering, University of North Carolina at Charlotte, Charlotte, North Carolina 28223

(Received 30 May 1989; accepted for publication 19 June 1989)

A high-current, nanosecond-pulse generator is described, ideal for driving low-impedance loads such as laser diodes. The generator utilizes step recovery diodes in a unique biasing scheme to produce 0.1–5 A pulses with pulse widths varying from 2 to 10 ns.

Optical fiber propagation studies such as high-resolution optical time domain reflectometry (OTDR) require short laser pulses. Typically, laser pulses between 2 and 10 ns wide are needed to resolve a fault location within a length of several meters. [1] The main objective of this work was to construct a relatively high-power semiconductor laser pulse generator with pulse width and current fully adjustable in the nanosecond regime. The other criteria were low-voltage power supply, small size, and the use of inexpensive off-the-shelf components. Avalanche-type generators are ruled out due to the difficulties involved in controlling pulse amplitude and width. [2] Normally, these parameters are adjusted by varying the distributed parameters of the avalanche circuit. Furthermore, the high avalanche breakdown voltages of most transistors produce considerable electromagnetic impulses when nanosecond switching occurs. This situation is especially undesirable when the laser pulse transmitter must be located in close proximity to a high-gain optical receiver. Shunt-series-type step recovery diode (SRD) pulsers have been in use for many years. These circuits are known for ease of adjustment and low-voltage operation.

SRDs can be used as charge-controlled switching elements, with transition times lower than 100 ps [3,4]. A forward-bias current is used to store charge in the diode. A reverse-bias signal is used to deplete the diode of stored charge. When depleted of stored charge, the SRD rapidly switches from a low-impedance state to that of high impedance. Figure 1 shows the classic shunt-series SRD pulse generator [5,6]. In this circuit, the SRD1 shunts the slowly rising edge of the incident pulse to the ground, depleting stored charge and preventing propagation of the pulse through the network. When the stored charge is depleted, SRD1 snaps off and presents a rapidly rising edge to the second stage of the network. SRD2 allows the pulse to pass through the load until the depletion of stored charge causes a rapid cutoff of current when the diode changes state.

The charge stored on a SRD from dc forward bias is given approximately by [6]

$$Q \approx I_b \tau, \tag{1}$$

where Q is the stored charge, I_b is the biasing current, and τ is the minority-carrier lifetime in the diode. Hence, bias current on SRD2 controls pulse width.

Using the SRD wave shaper to drive nonreactive 50 Ω loads is straightforward when standard microwave circuit construction rules are followed. Required bias currents for those loads are in the neighborhood of 10 mA. However, driving low-impedance high-current loads such as laser diodes can require dc bias currents exceeding 100 mA per diode [Fig. 1(a)]. Note the addition of Schottky diode D1 to prevent damaging reverse biases to the laser diode. Higher bias currents are necessitated by greater load currents, causing faster charge removal from the SRD junctions. Hence, for the same pulse width, a high-current circuit requires proportionately more bias current than a lower current pulse generator.

Fortunately, many nanosecond-pulse applications require low duty cycles. This allows a more efficient means of injecting charge into the SRDs, thus greatly reducing time-averaged bias current and its associated heat dissipation. Charge may be injected into the SRDs by a short, high-current bias pulse just before the incident pulse event (Fig. 2). Upon removal of the bias pulse, stored charge in the diode will decay with $\exp(-t/\tau)$, [6] and so the arrival of the main driving pulse in the network should be timed to arrive shortly after the bias pulse for maximum utilization of stored charge. It should be noted, however, that should the main pulse arrive during the bias period, pulse parameter adjustments will cease to be independent of each other due to cross

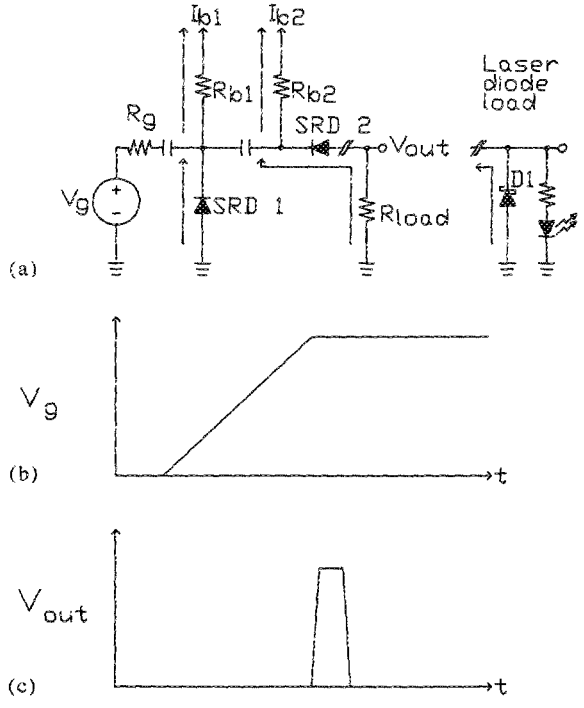

FIG. 1. Basic circuit diagram for a shunt-series-type step recovery diode pulse generator.

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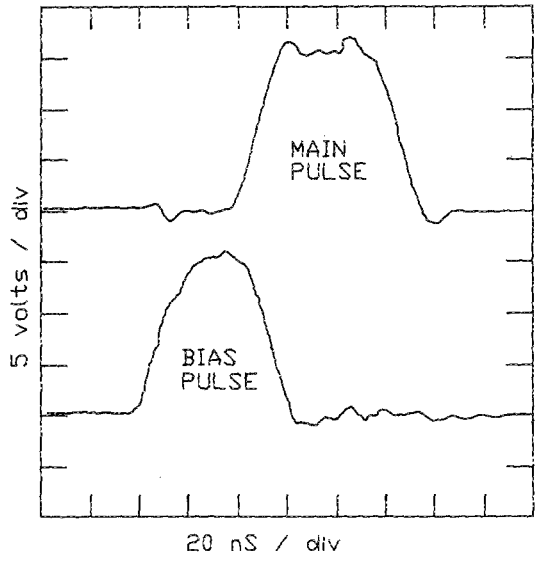

FIG. 2. Timing diagram showing application of bias pulse to SRDs.

flow of bias current from the shunt stage of the circuit to the series stage or vice versa. Timing of bias and main pulses is coordinated by an internal two-phase clock that is triggered in response to an input signal.

The pulse generator was constructed using readily available components (Fig. 3). The circuit was built on a 10-cm^2 ground plane with ordinary care taken to keep lead lengths short and stray inductances low. Application of a TTL trigger pulse to flip-flop U1 initiates pulse generation by producing a 50-ns bias pulse through the SRDs. Bias pulses are formed by discharging capacitors C1 and C2 through MOSFETS Q3 and Q4. The MOS transistors were type IRFF111, chosen for their rapid rise time characteristics. Any similar device may be substituted. MOSFETS are driven by U3, selected for its ability to rapidly charge the large gate capacitance of power MOSFET devices. Step recovery diodes SRD1 and SRD2 are M/A-COM 43-007, selected for their long minority-carrier lifetime and low package inductance. The bias pulse through SRD2 causes a small negative voltage to appear across the laser diode. Since diode lasers can be damaged by application of a reverse bias greater than 1 V, Schottky diode D1, a 1N5817, was selected to minimize this reverse bias and help control ringing in the output. Q2 isolates the bias currents through SRD1 and SRD2 so that pulse parameter adjustments may be made independently via potentiometer R1 and R2. As the bias pulse is decaying, the main driving pulse is being formed (Fig. 2). Capacitor C3 is discharged through Q1 providing a multiampere pulse with about 15-ns rise time to the charged step recovery diodes in the shaping network. Using a 4.7-Ω resistor for the load, a 2-A pulse can be generated (Fig. 4).

Using this circuit, a maximum peak voltage of around 10 V was obtained for loads ranging from 2 to 10 Ω. Current through the load was controlled by adjustments of VDD. Operation is satisfactory when VDD is between 0 and 12 V; higher voltages raise the source voltage of Q1 and Q2 beyond the drive capabilities of the MOS driver (DS0026). Note the negative-going prepulse event in Fig. 4, due to the charging of the step recovery diodes. Adjusting the width pot R2 controls the amount of stored charge on SRD2 and the width of the output pulse. Rise pot R1 controls the amount of charge on SRD1, affecting rise time and pulse delay. A maximum setting of this pot works well, reducing the setting when pulse overshoot is a problem. Total current consumption of the circuit was 70 mA, with a large 48-mA share of this going to power the MOS driver IC. SRD bias current for a 1 kHz PRF was under 4 mA, greatly reduced from the dc bias case.

Operation of the circuit with laser diodes is accomplished by using a suitable bandwidth series resistor to monitor laser current. The negative prepulse was small in magnitude and did not present any problems during operation.

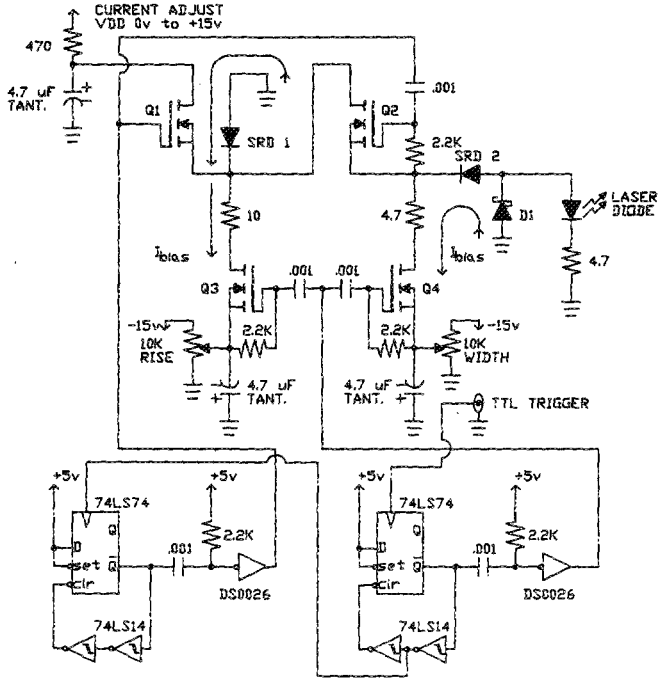

FIG. 3. Complete pulse generator with pulsed biasing scheme.

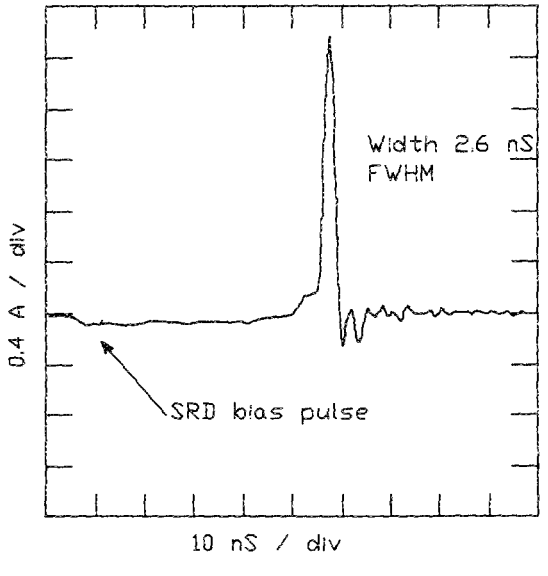

FIG. 4. Output of pulse generator into a 4.7 Ω resistive load.

Many high-power semiconductor laser diodes may be driven by this circuit.

In conclusion, the finished pulse generator met all of our original design criteria. Pulse parameters were adjustable not by physical changes to the circuit, but by potentiometer adjustments. No power supply voltages higher than 15 V need be used, reducing the amount of EMI generated. Finally, the circuit may be built on a 100-cm^2 area with ample room for laser diodes and other circuitry.

[1]S. D. Personick, Bell Syst. Tech. J. **56**, 355 (1977).
[2]S. I. Zienko, G. T. Pak, and V. Yu. Smerdov, Prib.Tech. Eksp. **27**, 100 (1984).
[3]Lloyd P. Hunter, *Handbook of Semiconductor Electronics*, 3rd ed. (McGraw-Hill, New York, 1970), Sec. 18 pp.6–13.
[4]J. A. Cockin, *High Speed Pulse Techniques* (Pergamon, New York, 1975), p. 133.
[5]*GE Transistor Manual*, 7th ed., 1964, GE Co.
[6]Pulse and Waveform Generation with Step Recovery Diodes, Hewlett Packard Application Note 918.

A simple implementation of a power supply for constant phototube current in light modulation spectroscopy

G. E. Jellison, Jr., and F. A. Modine

Solid State Division, Oak Ridge National Laboratory, P.O. Box 2008, Building 2000, MS 6056, Oak Ridge, Tennessee 37831-6056

(Received 8 May 1989; accepted for publication 9 June 1989)

A simple implementation of a commercially available high-voltage power supply is described whereby the power supply can be used for voltage biasing of a photomultiplier tube operating either in a constant dynode voltage or in a constant output current mode. In the constant current mode, low frequency fluctuations in the current are suppressed without attenuation of a high frequency signal. Both the phototube output current and the dynode voltage can be set by external voltages in the range from -10 to $+10$ V, making computer control easy with standard digital-to-analog converters.

In polarization modulation ellipsometry or polarimetry, as well as in many other applications involving photomultiplier tubes (PMTs), it is often desirable to maintain a constant dc current from the PMT while detecting the variations in a high-frequency signal. This is accomplished by changing the high voltage (i.e., the gain) of the PMT to compensate for slow variations in the light intensity incident upon the photocathode. Previous solutions[1–4] involved building a feedback control circuit to regulate a high-voltage power supply. In this note, we describe the much easier use of a commercial high-voltage operational power supply (Kepco OPS 1000B) which is implemented for this purpose, simply by strapping resistors to the rear programming terminals.

Figure 1 shows a schematic of the rear programming terminal and the output terminal of the Kepco OPS 1000B high voltage operational power supply (PS), along with the added resistors. A schematic diagram of the external resistors as well as many of the important internal components of the PS is shown in Fig. 2. In both figures, the circle with a central dot represent BNC connectors to input or output currents or voltages.

In the operation of this PS, the PMT output current is applied to a 10-kΩ load resistor and the voltage developed drives the resident uncommitted 741 operational amplifier of the PS. The 10-kΩ load is sufficiently small that a 100-kHz signal is not appreciably attenuated by the capacitance

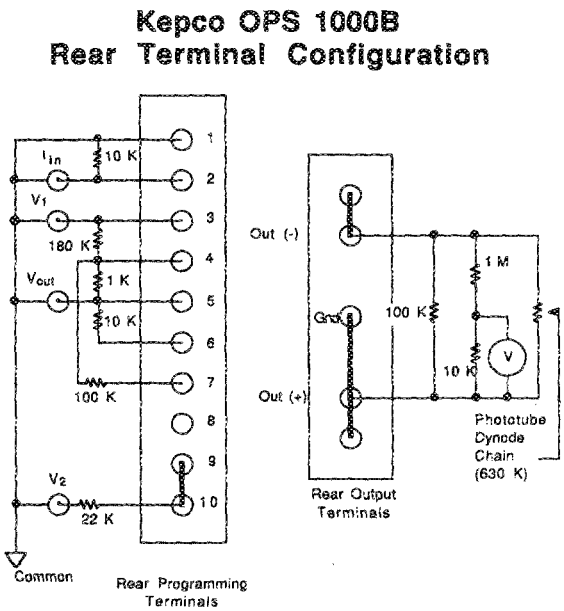

FIG. 1. Schematic diagram of the rear programming and rear output terminals of the Kepco OPS 1000B high-voltage power supply. Also shown are the programming resistor values used in our work, as well as the input and output voltages used for control of the bias voltage of the photomultiplier tube.

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