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1 GENERAL

1.1 Scope

This IceCube Engineering Requirements Document (ERD) document defines the requirements for the mechanical, electrical and functional interface between the Digital Optical Module main board (DOMMB) and the photomultiplier high-voltage base board (PMT HV Base board).

1.2 Purpose

This ERD is applicable to the development, prototyping, testing, and verification of the interface between the DOMMB and the PMT HV Base board.

1.3 Precedence

In the event of a conflict between the provisions of this document and any prior IceCube documentation, the provisions in this document shall supersede.

1.4 Responsibilities

1.4.1 IceCube Physics/Engineering is responsible for writing and updating these requirements to ensure they are correct, complete and current.

1.4.2 Quality Assurance is responsible for ensuring this document and changes to it are properly reviewed, approved and maintained.

1.5 Records

Records of initial review, approval and changes (Engineering Change Notices, ECN's) in design shall be maintained according to the established processes.

1.6 Units

Weights and measures in this document are expressed in the MKS International System of Units (SI).

1.7 Definitions

ADC	Analog-to-Digital Converter
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
CS0	Chip-Select Bit 0
CS1	Chip-Select Bit 1
DAC	Digital-to-Analog Converter
DOM	Digital Optical Module
DOMMB	Digital Optical Module Main Board

DAQ	Data Acquisition
ECN	Engineering Change Notice
ERD	Engineering Requirements Document
FWHM	Full-Width-at-Half-Maximum
HV	High Voltage
IDC	Insulation Displacement Connector
LSB	Least Significant Bit
MISO	Master-In-Slave-Out
MOSI	Master-Out-Slave-In
MSB	Most Significant Bit
ns	Nano-second (10^{-9} s)
OM	Optical Module
PCB	Printed Circuit Board
PMT	Photomultiplier Tube
SCLK	Serial Clock
SPI	Serial Peripheral Interface

2 FUNCTIONAL OVERVIEW

2.1 The Interface

The interface between the DOMMB and the PMT HV Base board (“interface”) consists of the following elements:

- **Physical interface** defines the requirements for the electrical cables between the DOMMB and the PMT HV Base board and the physical termination of the cables such as the requirements for connectors and soldering pads.
- **Electrical interface** defines the electrical signal assignment for the cables and any applicable electrical requirements for the said signals.
- **Functional interface** defines the logical protocols used by the DOMMB to communicate with the PMT HV Base board.

The physical connection between the DOM main board and the PMT HV Base board consists of the following three cabling media:

- Coaxial cable for connecting the anode pulse signals from the PMT HV Base board to the analog front-end of the DOM main board.

- Ribbon cable for the digital communication between the two boards and for the ± 5 volt power and digital ground connections.
- An insulated stranded wire for making the clean analog ground connection.

2.2 DOM Main Board (DOMMB)

Being the master controller of the entire Digital Optical Module (DOM), the Digital Optical Module Main Board (DOMMB) interfaces with a number of components both inside and outside the DOM. For the purpose of this ERD, the DOMMB serves the following functions:

- Provides electrical power to the PMT HV Base board
- Digitizes the analog pulses received from the PMT HV Base board
- Digitally controls and monitors the PMT HV Base board via serial communication

2.3 PMT HV Base Board

The PMT HV Base board facilitates the following functions:

- Generate a series of high voltages used to operate the photomultiplier tube (PMT) using the electrical power provided by the DOMMB.
- Transfers the anode signal pulses without significant distortion from the PMT to the DOMMB through a coaxial cable.
- Responds to the digital control commands issued by the DOMMB for (1) power ON/OFF; (2) high-voltage adjustment; (3) high-voltage readout; and (4) digital board identification.

3 THE INTERFACE REQUIREMENTS

3.1 Power

The DOM main board shall provide **± 5 VDC** power and power ground connection to the PMT HV Base board through the ribbon cable (below).

3.1.1 The power consumption by the PMT HV Base board shall be no greater than **150 mW**.

3.2 Ground

The PMT HV Base board shall have a split-ground configuration, consisting of the digital-and-power ground and the clean analog ground, as specified in the PMT HV Base Board ERD (**Figure 3.1**).

3.2.1 Digital and power ground connection

The digital-and-power ground shall be connected to the corresponding ground of the DOMMB through the ribbon cable (below).

3.2.2 Clean analog ground connection

The clean analog ground shall be connected between the PMT HV Base board and the DOMMB using a designated wire.

3.2.2.1 The PMT HV Base board and the DOMMB shall each have a wire-soldering pad on board for this purpose.

3.2.2.2 The said designated wire shall be a 20-AWG stranded wire (0.52mm^2) of **<TBD>** cm in length (see Section 4), whose ends are directly soldered to the wire-soldering pads.

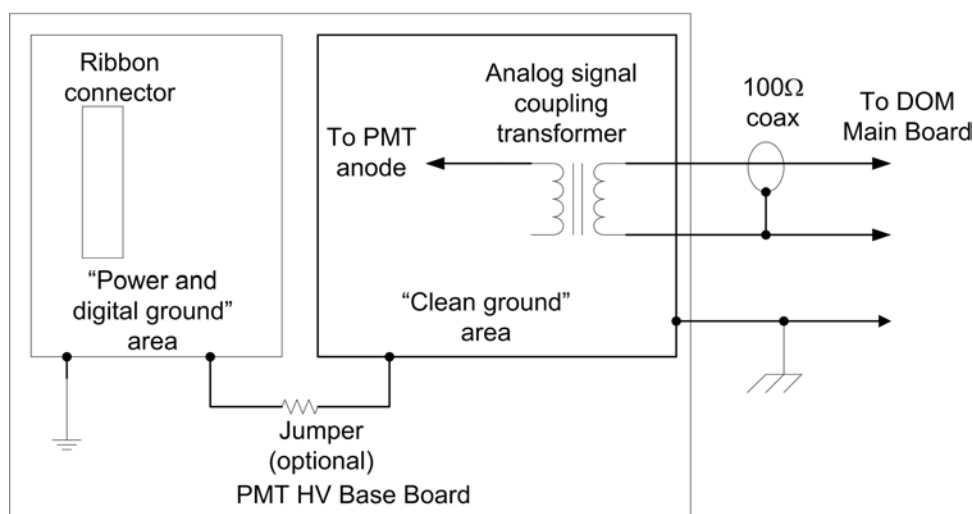


Figure 3.1 Split ground configuration requirement

3.3 PMT Anode Signal

3.3.1 Analog signal gain and dynamic range

The gain setting of the PMT HV Base board shall be such that 200 photoelectrons (PEs) occurring over a 15 ns time interval in the PMT produces a voltage pulse of 1 V in amplitude into the $100\ \Omega$ load at the DOMMB analog front-end.

3.3.2 Signal connection

The connection of the anode transformer secondary to the DOM main board shall be made using RG-180B/U coaxial cable or other suitable coaxial cable with a similar characteristic impedance (100Ω).

3.3.3 Method of connection

The coaxial cable shall be connected to the DOMMB by direct soldering.

3.4 Ribbon Cable Connection

3.4.1 Cable Type

The ribbon cable shall be of a 1mm-pitch IDC type with twenty (20) conductors and shall have a 2mm male connector (IDC type with a polarization key) on each end.

3.4.2 Connectors

The PMT HV Base board and the DOMMB shall each have a female ribbon cable receptacle for the ribbon cable connection.

3.4.2.1 The pin spacing and the number of pins of the said receptacle shall be consistent with the requirements in **3.4.1**.

3.4.3 Ferrite Core Requirement

The ribbon cable shall be threaded through a ferrite core before the last connector is affixed to it. The ferrite core shall be glued to the cable at a location least likely to cause any mechanical problems.

<The said location shall be determined experimentally by IceCube engineers and be defined as a requirement in a later revision of this document. In the event that the ferrite core is found to be unnecessary by the said experimentation, this document shall be revised to reflect such a finding.>

3.4.4 Signal Duplication Requirement

Each signal, ground and power lead in the ribbon cable shall have two connector pins allocated to it.

3.4.5 Ribbon Connector Signal Assignment

The signal name assignment on the individual pins on the ribbon connector shall be according to the definition in **Table 3.1**.

Table 3.1 Ribbon connector signal assignment

Pin #	Signal name	Description
01	DGND	Digital and power ground
02	SCLK	Serial clock
03	SCLK	
04	MOSI	Master-out-slave-in
05	MOSI	
06	MISO	Master-in-slave-out
07	MISO	
08	DGND	
09	CS0	Chip-select bit 0
10	CS0	
11	CS1	Chip-select bit 1
12	CS1	
13	ON/OFF	Board power ON/OFF
14	ON/OFF	
15	+5V	Main power (+)
16	+5V	
17	DGND	
18	DGND	
19	-5V	Main power (-)
20	-5V	

3.5 Digital Interface

3.5.1 Digital Signal Standard

The digital signals (logic levels and voltages) between the PMT HV Base board and the DOMMB shall comply with the **3V CMOS** signal standard.

3.5.1.1 Neither the PMT HV Base Board nor the DOMMB shall rely on the 5V-tolerance of the receiver when transmitting a signal.

3.5.2 Power ON/OFF control

The main power on the PMT HV Base board shall be turned on or off by controlling the ON/OFF signal as described in Table 3.2.

Table 3.2 ON/OFF signal assignment

Logic Level	Meaning
0	OFF
1	ON

3.5.3 Power-up default

When the PMT HV Base board is turned on, the HV output shall be consistent with the DAC digital code of 0x000 (See **3.5.5**).

3.5.4 Device Assignment to the Ribbon Cable Signals

<The assignment of the digital communication signals on the ribbon cable (SCLK, MISO, MOSI, CS0, CS1) to the individual ports of the digital devices residing on the PMT HV Base board shall be defined in a revision of this document at a later date when the design of the PMT HV Base Board is approved by IceCube. The said revision shall also define, as necessary, the protocols for operating the DAC, the ADC and the IDENT device by DOMMB.>

Note: In accordance with the PMT HV Base Board ERD, the vendor of the PMT HV Base board shall meet the following requirements regarding the assignment of the digital communication signals on the ribbon cable:

3.5.4.1 **Chip-select** - The two chip-select signals, CS0 and CS1, shall be used in combination to select one of the following three digital devices residing on the PMT HV Base board:

- DAC: Digital-to-analog converter
- ADC: Analog-to-digital converter
- IDENT: Board identification device

3.5.4.2 The assignment of the logic levels to CS0 and CS1 shall be determined by the vendor of the PMT HV Base board.

3.5.4.3 **MOSI, MISO and SCLK signals**

- DAC shall use MOSI and SCLK for data and serial clock, respectively.
- ADC shall use MISO and SCLK for data and serial clock, respectively.
- IDENT shall use one or more of MOSI, MISO and SCLK, according to the vendors implementation of the PMT HV Base board.

3.5.5 Digital high-voltage control (DAC)

The digital-to-analog converter (DAC) residing on the PMT HV Base Board for the purpose of controlling the high-voltage output value shall comply with the SPI™ protocol.

3.5.5.1 The digital code shall be 12-bit unsigned straight binary.

3.5.5.2 The scaling between the digital code written to the DAC and the high-voltage produced by the PMT HV Base Board shall be 0.5 V per bit over the valid range specified in the PMT HV Base Board ERD.

3.5.6 Digital high-voltage monitor (ADC)

The analog-to-digital converter (ADC) residing on the PMT HV Base Board for the purpose of monitoring the high-voltage output value shall comply with the SPI™ protocol.

3.5.6.1 The digital code shall be 12-bit unsigned straight binary.

3.5.6.2 The scaling between the digital code read from the ADC and the high-voltage being monitored shall be 0.5 V per bit over the valid range specified in the PMT HV Base Board ERD.

3.5.7 Digital board identification (IDENT)

The digital board identification device residing on the PMT HV Base board shall comply with the Dallas 1-Wire™ protocol to communicate with DOMMB that serves as the bus master.

4 MECHANICAL REQUIREMENTS

<Relative orientation of the DOMMB PCB and the PMT HV Base Board PCB, the locations of the relevant connectors, and the lengths of the cables shall be documented in the earliest revision of this ERD.>

5 REFERENCES

- DOM Main Board ERD
- PMT HV Base Board ERD