DOM Main Board "Getting Started" Manual*

Version 0.02

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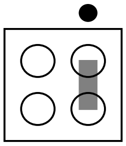
Preparation

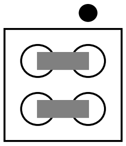
- Power connection (40 – 120 VDC)
  - Connect (+) to TB1/TB3
  - Connect (-) to TB2/TB4

- Enable serial port communication by setting jumper JP18

- Set jumper JP2



➔Allows flash memory programming



➔For re-programming serial PROM only

- Ribbon connectors to PC parallel port (optional)
  - Use JP3 to program the CPLD (Xilinx Cool Runner II)
  - Use JP10 to program the XCALIBUR Flash Memory and EPC II (serial PROM)
  - To program the Xilinx part, an adapter must be inserted in the cable. See the following link for the adapter. http://rust.lbl.gov/~gtp/DOM/Support/JTAG Adapter.pdf

- Set up the serial communication
  - Use Hyper Terminal or any similar terminal program.
  - Emulate VT100, 115.2K Baud, 8N-1, Hardware handshake
  - The serial connection is made with an RJ45 (Ethernet) cable between JP17 and the PC COM port. This requires an adapter (DB9 female to RJ45), which can be purchased from http://cablesonline.com. For the pinouts, see

http://rust.lbl.gov/~gtp/DOM/Support/Serial_Cable_pin-out.pdf.

- Connect the serial cable and turn on the power. The Hyper Terminal window should now show “Ready…” followed by the prompt “>”.

❖ Load FPGA vial serial cable

- At the prompt, type “ymodem1k” (case sensitive)➔ Now the FPGA enters a “receive mode”.
- Under the Hyper Terminal menu, select “Transfer”. In the popup window, select Ymodem and enter the filename (*.sbi) to download. The most current binary file is available from http://deimos.lbl.gov/~arthur/bin/simpletest_ver2_5.sbi.
- Click “Send”➔At this point, the data stream is stored in the CPU memory.
- At the prompt, enter “fpga”➔Now the data are transferred to the FPGA.
- Verify the operation by entering the “print stack” command (“.s”) and examining the value on the top of the stack. If it is zero, the operation has been successful.

Important addresses, bits, and how to find them

- Consult the documents in the following pages:
  http://rust.lbl.gov/~gtp/DOM/API/index.html
  http://deimos.lbl.gov/~arthur/dom-mb/modules.html
- Hexadecimal numbers are prefixed by a “$” sign for commands.
- Depending on the functions to be executed, an appropriate base address must be used.
  - DOMMB CPLD base address ➔ $50000000
  - Flasher CPLD base address ➔ $60000000
  - DOMMB FPGA base address ➔ $90000000

Data acquisition

❖ Setting up DAC values

- In order to perform data acquisition, various analog control voltages must be set up. Each ATWD, for example, requires four control voltages. The table shows the most current default values.

Table I

Purpose	**DAC #**	**Value**
ATWD #0	0	850

ATWD #0	1	2097
ATWD #0	2	3000
ATWD #0	3	2048
ATWD #1	4	850
ATWD #1	5	2097
ATWD #1	6	3000
ATWD #1	7	1925
???	8	
SPE discriminator	9	486
???	10	
FADC reference	11	700
Test pulser amplitude	12	

- ❖ Select data acquisition mode
  - The relevant register address is obtained by looking up various tables.

    ```
    #define DOM_FPGA_TEST_BASE    (DOM_FPGA_BASE + 0x00080000)
    #define DOM_FPGA_TEST_LOCAL   (DOM_FPGA_TEST_BASE + 0x1008)
    ```

    See, for example,

    http://deimos.lbl.gov/~arthur/dom-mb/group_fpga_test_local.html

    The first entry is the register address, and the rest is the 32-bit values corresponding to various modes and functions.
  - Forced-trigger mode→The data capture takes place upon entering command

    ```
    >$10000 $90081008 !
    ```

    (→ATWD#0)
  - Discriminator mode→The discriminator is used to trigger the data aquisition

    ```
    >$20000 $90081008 !
    ```

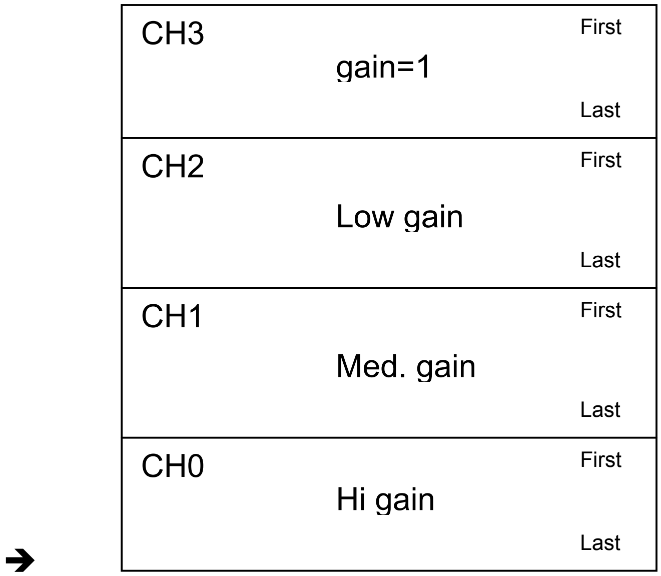
    (→ATWD#0)
- ❖ Check for "done" bit (bit 16 for ATWD#0) by the command:

  ```
  >$9008100c @ .
  ```

- ❖ View data by "octal dump" command:

  ```
  >$90084000 512 od
  ```

  (→ATWD#0)
  - Bits 0-9 contain data. Bits 10-31 are filled with zero.
  - The 10-bit data words are arranged in the format shown below.



Base + $4000 for ATWD#0
Base + $5000 for ATWD#1

- ATWD Trivia
  - "Pedestal noise"—constant noise characteristic of individual ATWD. This noise must be measured and subtracted from actual data.
  - The first set of digitized data, either after the power-up or after an extended period (several seconds) of idling, is invalid and must be discarded.

- Additional documentation (essential reading)
  - Arthur Jones, "Iceboot Users Guide", May 14, 2003
    http://deimos.lbl.gov/~arthur/dom/

Command Examples

- Turn on PMT HV Base Board
  Set bit 0 of External Module Control Register (DOMMB CPLD base + $F9) by writing a character to the register:

```
> 1 $500000F9 c!
```

- Turn off PMT HV Base Board

```
> 0 $500000F9 c!
```

- Set PMT Base High Voltage—nn is the value between 0 and 4095. The current firmware has two separate commands:

```
> nn writePassiveBaseDAC

> nn writeActiveBaseDAC
```

- Read PMT Base High Voltage value—Use the period "." to print the top of the stack.

```
> readBaseADC .
```

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*From the notes made by N.K. during his visit to LBNL (4/29-5/2/03).
Thanks to Thorsten Stezelberger!